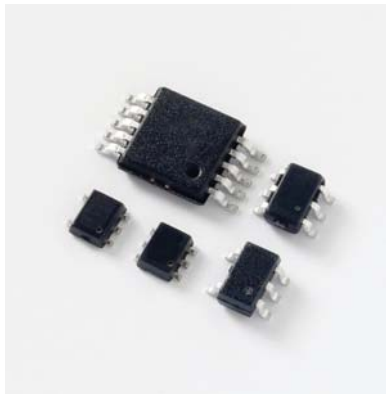
Littelfuse®

Expertise Applied | Answers Delivered

PRODUCT CATALOG & DESIGN GUIDE



SPA™

TVS Diode Array Products for ESD and Lightning Protection

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DESIGN SUPPORT

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Product Sampling Programs—Most of our products are available as samples for testing and verification within your circuit design. Visit Littelfuse.com or contact a Littelfuse product representative for additional information.

Product Evaluation Labs and Services—Littelfuse global labs are the hub of our new product development initiatives, and also provide design and compliance support testing as an added-value to our customers.

OVERVOLTAGE SUPPRESSION TECHNOLOGIES (1-6)

1. TVS Diodes — Suppress overvoltage transients such as Electrical Fast Transients (EFT), inductive load switching and lightning in a wide variety of applications in the computer, industrial, telecom and automotive markets.

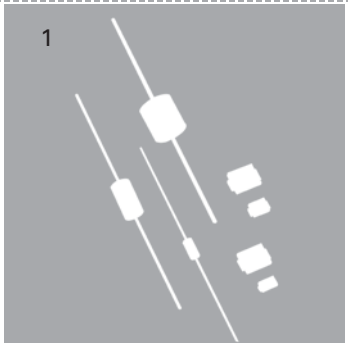
2. Varistors — Multiple forms, from Metal Oxide Varistors (MOVs) that suppress transient voltages to Multi-Layer Varistors (MLVs) designed for applications requiring protection from various transients in computers and handheld devices as well as industrial and automotive applications.

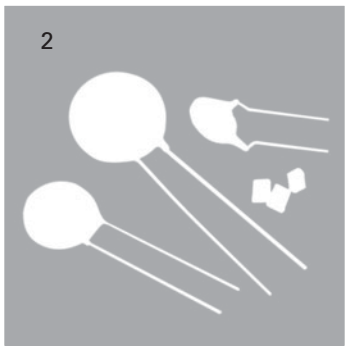
3. SIDACtor® Devices— Complete line of protection thyristor products specifically designed to suppress overvoltage transients in a broad range of telecom and datacom applications.

4. Gas Plasma Arrestors (GDTs) — Available in small footprint leaded and surface mount configurations, Littelfuse GDTs respond fast to transient overvoltage events, reducing the risk of equipment damage.

5. TVS Diode Arrays (SPA™ Family of Products)— Designed specifically to protect analog and digital signal lines from electrostatic discharge (ESD) and other overvoltage transients.

6. PulseGuard® ESD Suppressors — Available in various surface mount form factors to protect high-speed digital lines without causing signal distortion.





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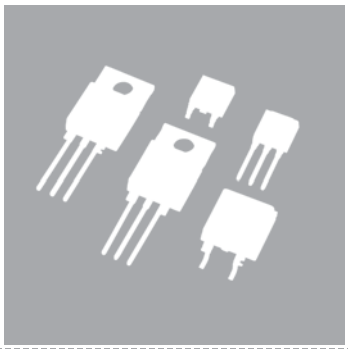
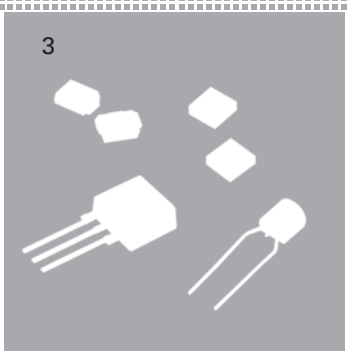
SWITCHING TECHNOLOGIES

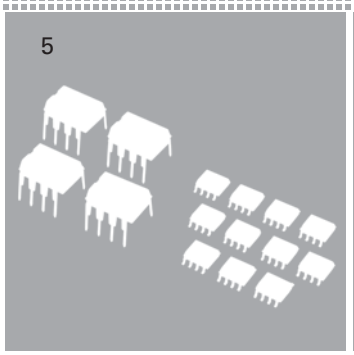
Switching Thyristors— Solid-state switches used to control the flow of electrical current in applications, capable of withstanding rated blocking/off-state voltage until triggered to on-state.

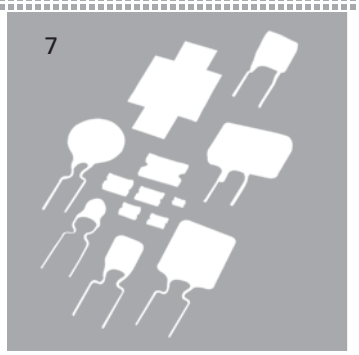
SPECIAL APPLICATION PRODUCTS

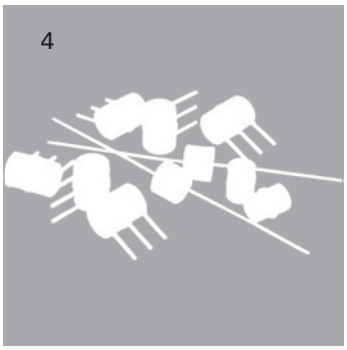
PLED LED Lighting Reliability Devices — Specialty silicon devices that enable LED lighting strings to continue to function if any single LED fails as an open circuit, and also offer ESD and reverse power protection.

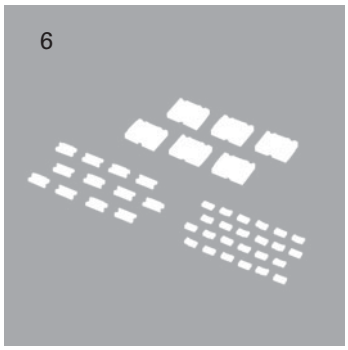












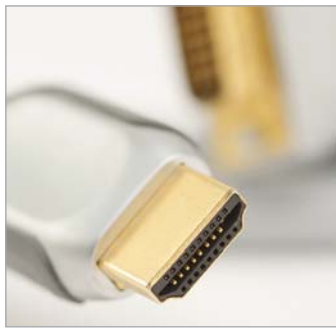
OVERCURRENT PROTECTION TECHNOLOGIES (7-8)

7. Positive Temperature Coefficient Devices (PTCs)— Provide resettable overcurrent protection for a wide range of applications.

8. Fuses — Full range including surface mount, axial, glass or ceramic, thin-film or Nano$^{2®}$ style, fast-acting or SloBlo®, MINI® and ATO® fuses.

www.littelfuse.com for more information.











Circuit Protection with SPA™ TVS Diode Arrays

Littelfuse Silicon Protection Array (SPA™) Family of TVS Diode Arrays are designed to protect electronics from very fast and often damaging voltage transients, such as lightning and electrostatic discharge (ESD). They offer an ideal protection solution for I/O interfaces and digital and analog signal lines, in computer and consumer portable electronics markets.

Littelfuse SPA Devices are available in a range of packaging configurations including DIP, SOIC, MSOP, SOT23, SOT143, SC70, SOT5x3, SOT953, µDFN, SOD723, and flipchip.

Features

- Low capacitance of 30pF to 0.40pF typically
- High level of protection:
  - ESD IEC 61000-4-2; Contact discharge up to ±30kV; Air discharge up to ±30kV
  - Lightning, IEC 61000-4-5; Immunity up to 150A
  - EFT IEC 61000-4-4 40A (5/50ns)
- Low clamping voltage compared to other technologies
- Up to 14 inputs protection
- Space saving arrays and ultra-small 0201 and 0402 devices for mounting close to ports for optimal protection
- ROHS compliant, Pb-Free and Halide-free for most devices

Visit www.littelfuse.com/SPA for more information.

CONTENTS

Series Name[1]	Photo	Package Type	Working Voltage	Resistance	Capacitance	Number of Channels	ESD Rating (Contact Discharge, IEC61000-4-2)	Clamping Voltage (T_P=8/20µs)	Cut Off Frequency	Peak Current (T_P=8/20µs)	Green	Lead Free	RoHS	
General Purpose ESD Protection - Protection for human interfaces (keypads, buttons, switches, audio ports, etc)														
SP05		SC70, SOT23, SOT143, MSOP	5.5V		30pF	2 / 3 / 4 / 5 / 6	30kV				•	•	•	15
SP1001		SC70, SOT553 SOT563	6V		8pF	2 / 4 / 5	15kV	8.0V@1A		2 A	•	•	•	21
SP1002		SC70	6.5V		5pF	1 / 2	8kV	9.2V@1A		2 A	•	•	•	27
SP1003		SOD723	5V		30pF	1	30kV	12V@7A		7 A	•	•	•	31
SP1004		SOT953	6V		5pF	4	8kV	10V@1A		1 A	•	•	•	35
SP1005		0201 (Flipchip)	6V		30pF	1	30kV	9.3V@1A		10 A	•	•	•	39
SP1007		0201 (Flipchip)	6V		3.5pF	1	8kV	10.3V@1A		2 A	•	•	•	43
SP1010		µDFN	6V		3.5pF	4	8kV	9.8V@1A		1 A	•	•	•	47
SP1011		µDFN	6V		7pF	4	15kV	8.7V@1A		2 A	•	•	•	51
SP720		PDIP, SOIC	2-30V		3pF	14	4kV	2V@1A		3 A	•	•	•	55
SP721			2-30V		3pF	6	4kV	2V@1A		3 A	•	•	•	61
SP723			2-30V		5pF	6	8kV	2V@2A		7 A	•	•	•	67
SP724		SOT23	1-20V		3pF	4	8kV	2V@1A		3 A	•	•	•	73
SP725		SOIC	2-30V		5pF	4	8kV	2V@2A		14 A	•	•	•	79
Low Capacitance ESD Protection - Protection for data lines (USB, HDMI, eSata, etc)														
SP3001		SC70	6V		0.65pF	4	8kV	9.5V@1A		2.5 A	•	•	•	85
SP3002		SC70, SOT23,µDFN	6V		0.85pF	4	12kV	9.5V@1A		4.5 A	•	•	•	89
SP3003		SC70, SOT5x3, MSOP10	6V		0.65pF	2 / 4	8kV	10.0V@1A		2.5 A	•	•	•	95
SP3004		SOT563	6V		0.85pF	4	12kV	10.0V@1A		4 A	•	•	•	101
SP3010		µDFN	6V		0.45pF	4	8kV	10.8V@1A		3 A	•	•	•	105
SP3011		µDFN	6V		0.40pF	6	8kV	11.0V@1A		3 A	•	•	•	109
Lightning Surge Protection - Protection for broadband data and communication lines (Ethernet, xDSL, etc)														
SP03-3.3		SOIC	3.3V		16pF	2	30kV	15V@100A		150 A	•	•	•	113
SP03-6		SOIC	6V		16pF	2	30kV	20V@100A		150 A	•	•	•	117
SPLV2.8		SOT23	2.8V		2.1pF	1	30kV	15V@24A			•	•	•	121
SPLV2.8-4		SOIC	2.8V		2.1pF	4	30kV	15V@24A			•	•	•	125
SP3050		SOT23	6V		2pF	4	20kV	8.8V@1A		10 A	•	•	•	129
SP4060		MSOP	2.5V		4.4pF	8	30kV	4.5V@1A		20 A	•	•	•	133
ESD and EMI Filter Devices - Protection for mobile device display interfaces (mobile phones, navigation devices, etc)														
SP6001		µDFN	6V	100Ω	24pF	4 / 6 / 8	30kV		115MHz		•	•	•	137
SP6002		µDFN	6V	100Ω	30pF	4 / 6	30kV		100MHz		•	•	•	141

TVS DIODE ARRAY TECHNOLOGY AND APPLICATIONS OVERVIEW

Introduction to TVS Diode Array (SPA™) Devices

Littelfuse Silicon Protection Array (SPA™) family of TVS Diode Arrays are designed to protect analog and digital signal lines, such as USB and HDMI, from various transient threats using the lowest possible clamp voltage. They offer broader application use and improved impulse protection performance over conventional diodes.

These robust devices safely absorb repetitive ESD strikes at the maximum level (Level 4) specified in the IEC 61000-4-2 international standard, without performance degradation.

Key Features

- Low capacitance 30pF to 0.40pF typically
- High level of protection:
  - ESD IEC 61000-4-2: Contact discharge up to ±30kV; Air discharge up to ±30kV
  - Lightning, IEC 61000-4-5; Immunity up to 150A
  - EFT IEC 61000-4-4 40A (5/50ns)
- Low clamping voltage compared to other technologies
- Up to 14 inputs protection
- Space saving arrays and ultra-small 0201 and 0402 devices for mounting close to ports for optimal protection
- ROHS compliant, Lead-Free and Halogen-Free devices

How they Work?

Littelfuse TVS Diode Array devices provide high level protection against Electrostatic Discharge (ESD), Electromagnetic Interference (EMI) and Lightning, mainly for sensitive digital and analogue input circuits, on data, signal, or control lines operating on power supplies.

These devices work in two ways. First, they absorb transients with diodes, to steer the current, and then, an avalanching or zener diode, clamps the voltage levels. This prevents the device from exceeding its voltage rating. During over-voltage fault conditions, the device must have a low clamp voltage at the specified current wave form to protect sensitive IC's and ports.

In normal operation, the reverse stand off voltage must be higher than the equipment supply/working voltage, with low leakage current to prevent power supply loading. The device capacitance must be low enough to reduce input signal distortion. The device package must have a small footprint and low height to enable a high density Printed Circuit Board (PCB) layout.

The device must withstand multiple ESD pulses as specified in the IEC 61000-4-2.

Data Protocols and End Applications

The diagrams on the next page show the relationship between Data Rates (Protocol), Applications, and Littelfuse TVS Diode Array (SPA™) Devices.

The top diagram shows the standard data protocols, associated data rates, example end applications, and applicable Littelfuse SPxxxx device series. Similarly, the bottom diagram shows common end applications and applicable SPxxxx devices in table format.

This information, along with the example circuit protection configuration diagrams on the following pages, and within each data sheet, is intended to help circuit designers determine which Littelfuse suppressors are most appropriate for the situation.

Most electronic products today use several port and data protocol types, and so require multple strategies of protection at each possible ESD transient entry point.

Concern About Capacitance

As data rate and data integrity concerns increase, so should concern about the capacitance of the suppression device.

For example, audio and mouse ports on most PCs use relatively slow data rates where capacitance of the ESD protector is not very important.

However, in today's higher bandwidth applications, the designer must be very conscientious about the parasitic capacitance of the protection device, to ensure that it does not cause signal degradation at very high frequencies.

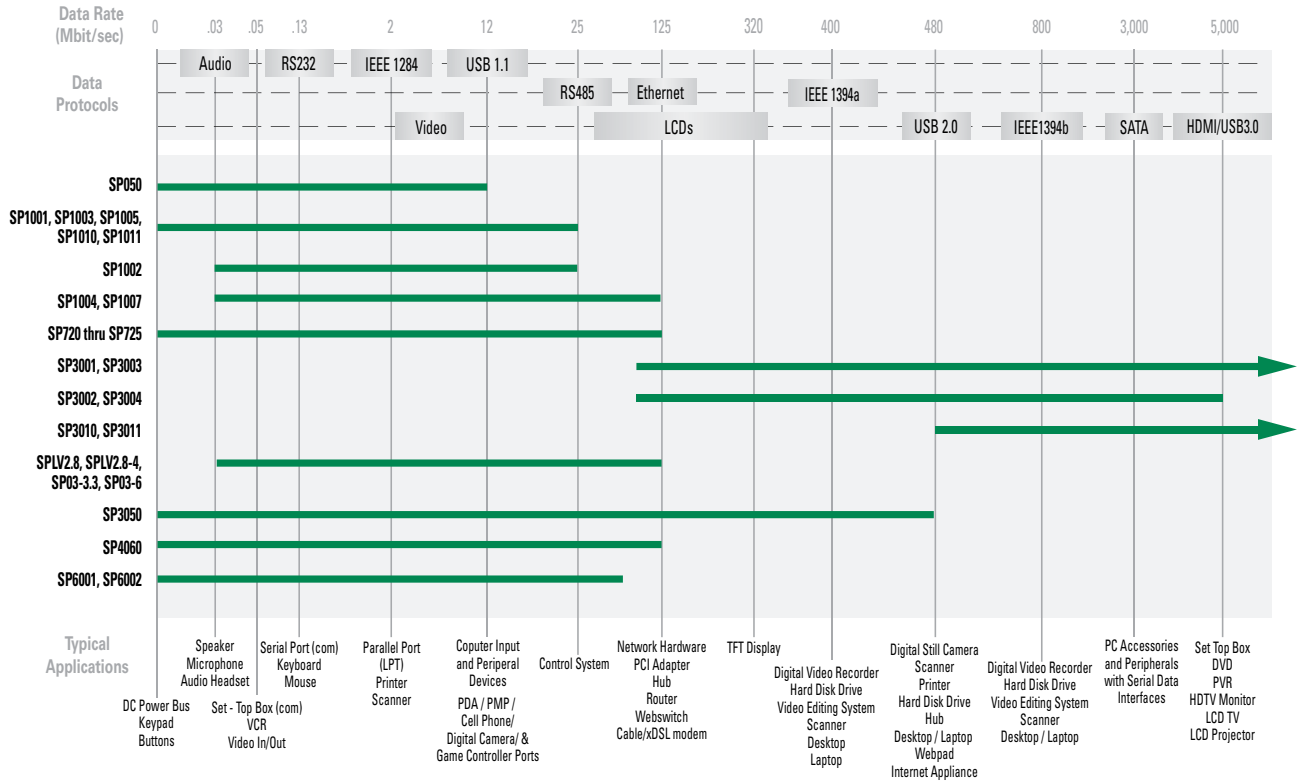
As data rates have continued to push higher (e.g. USB3.0, Gigabit Ethernet, HDMI, etc) chipsets have become more sensitive to ESD and other electrical transients by virtue of their small geometry processing. The only technology currently capable of preserving signal integrity and providing very low clamping voltages are Littelfuse SPA devices.

Other key characteristics such as leakage current, number of lines of protection, ESD immunity, and footprint also need to be considered, especially where there are overlaps in the recommended Littelfuse ESD suppressor line.

If you require further assistance in selecting the appropriate Littelfuse ESD suppressor for your specific circuit, please contact your local Littelfuse products representative.

For additional information including reference design examples, please visit www.littelfuse.com/SPA

SPxxxx PRODUCT SERIES AND APPLICABLE DATA RATES AND PROTOCOLS



SPxxxx PRODUCT SERIES AND RELATED END APPLICATIONS

Product Series	SP050X	SP1001	SP1002	SP1003	SP1004	SP1005	SP1007	SP1010	SP1011	SP720	SP721	SP723	SP724	SP725	SP3001	SP3002	SP3003	SP3004	SP3010	SP3011	SP03-3.3	SP03-6	SPLV2.8	SPLV2.8-4	SP3050	SP4060	SP6001	SP6002
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Audio Lines	X	X	X	X	X	X	X	X	X																			
Low speed I/O Port	X	X	X	X	X	X		X	X	X	X	X	X	X									X		X			
USB 1.1 Port	X	X						X	X																X			
USB 2.0 Port															X	X	X	X							X			
USB 3.0 Port																			X	X								
1394 Port															X	X	X	X	X									
HDMI Port															X	X	X	X	X									
LCD Display Monitors	X	X			X			X	X						X	X	X	X								X		
Handheld Device LCD Display																											X	X
SIM Socket	X	X		X		X	X	X	X																			
Memory Card Interface	X	X		X	X			X	X																			
Keypads/Buttons	X	X		X	X	X	X	X	X																			
Analog Video	X	X	X	X	X	X	X	X	X																			
Ethernet Port															X	X	X	X			X	X	X	X	X	X		

NOTE: The application summaries listed here are for reference only. Determination of suitability for a specific application is the responsibility of the customer.

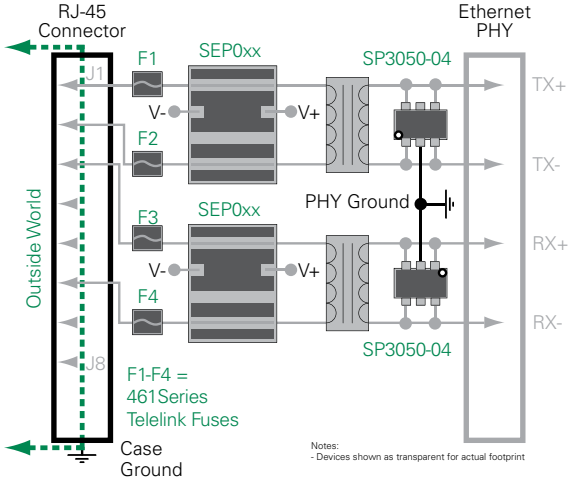
PORT PROTECTION EXAMPLES

BROADBAND NETWORK PORT PROTECTION

The following are examples of the implementation of ESD and lightning suppression for Ethernet ports (RJ-45 connectors). Note that the diagrams shown below represent 10Mbps and 100Mbps applications -- For 1Gbps applications, the circuit protection should be double of what is shown. For additional design examples, guidance and application assistance, please contact Littelfuse.

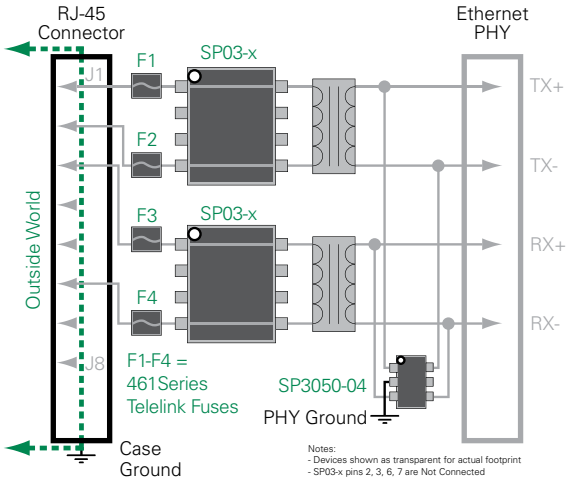
Inter-Building - Robust Lightning Protection

The diagram show below is typical for outdoor network line and equipment applications. The SIDACtor® and TVS Diode Array combination is rated up to 500A, per the GR-1089 standard.



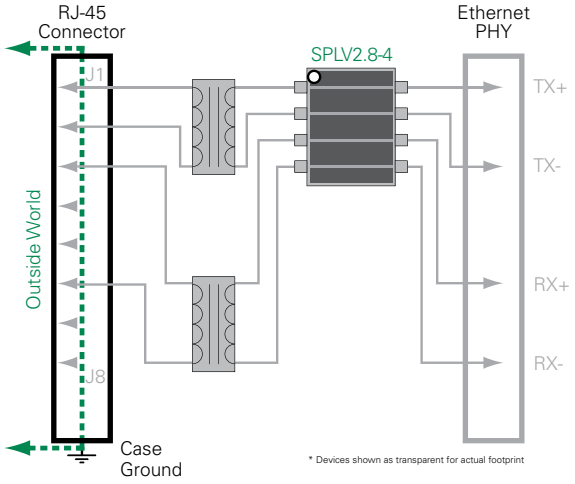
Intra-Building - Robust Lightning Protection

The diagram show below is typical for indoor network line and equipment applications. The TVS Diode Array device combination is rated up to 100A, per the GR-1089 standard.



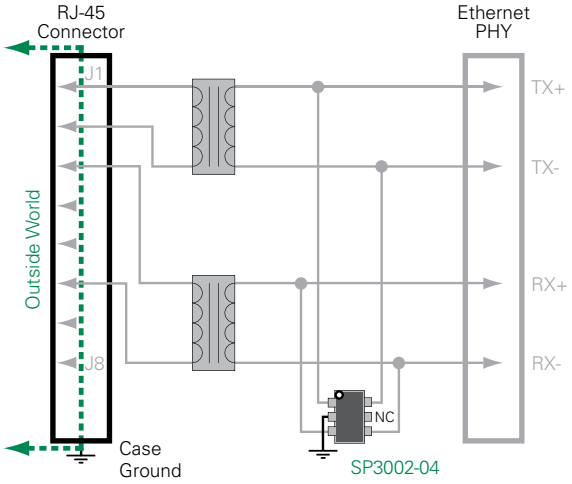
Basic Lightning Protection

The diagram shown below is typical for basic lightning (differential only) of indoor/outdoor network line and equipment applications (Example: office environment equipment).



Basic ESD Protection

The diagram shown below is typical for basic ESD protection of indoor network line and equipment applications (Examples: home office / consumer electronics peripheral devices).

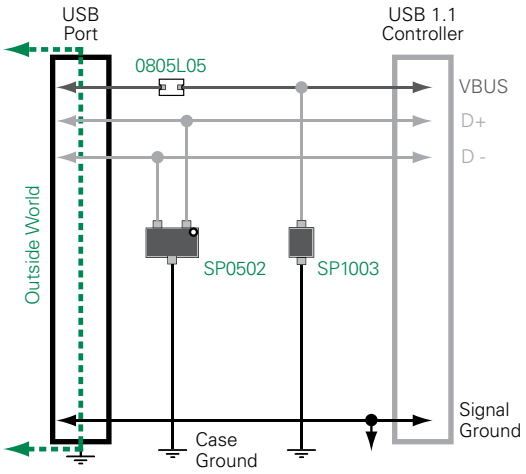


PERIPHERAL / STORAGE DATA PORT PROTECTION

The following are examples of ESD suppression for high speed data ports such as USB and eSATA. For additional design examples, guidance and application assistance, please contact Littelfuse.

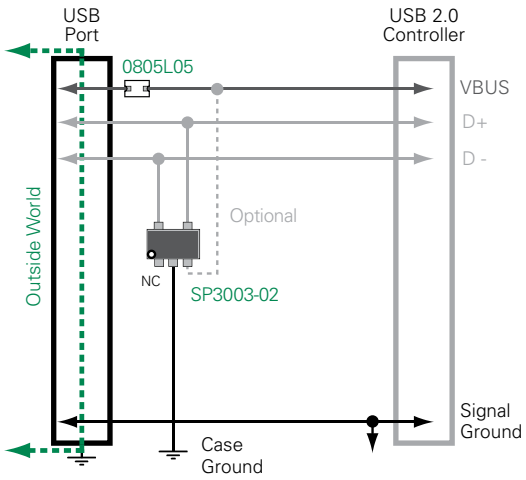
USB 1.1

Data speeds up to 12 Mbps



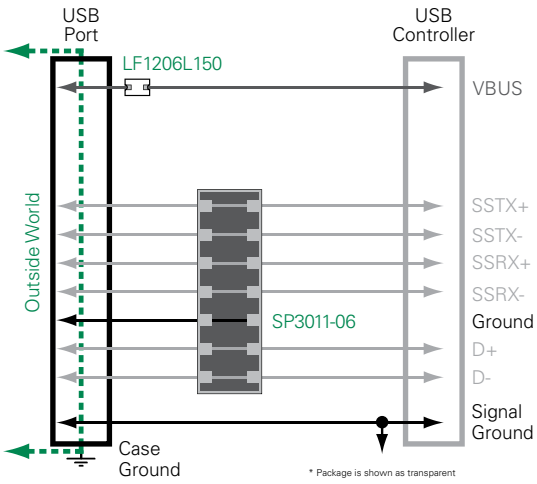
USB 2.0

Data speeds up to 480 Mbps



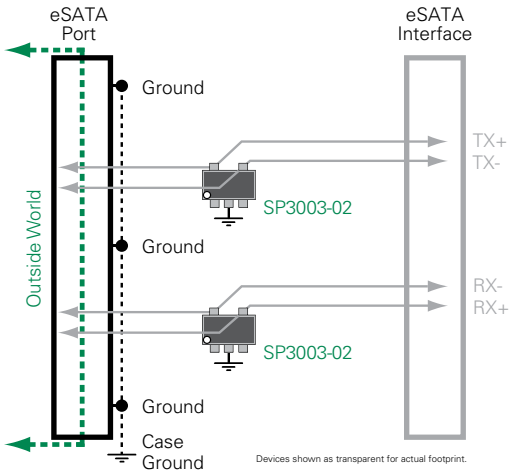
USB 3.0

Data speeds up to 5 Gbps



eSATA

Data speeds up to 3 Gbps

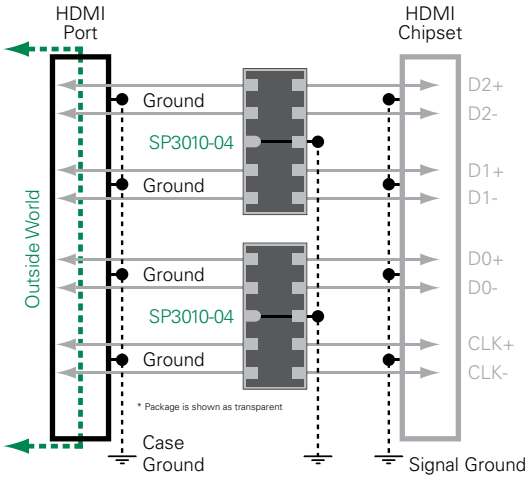


ENTERTAINMENT ELECTRONICS PORT PROTECTION

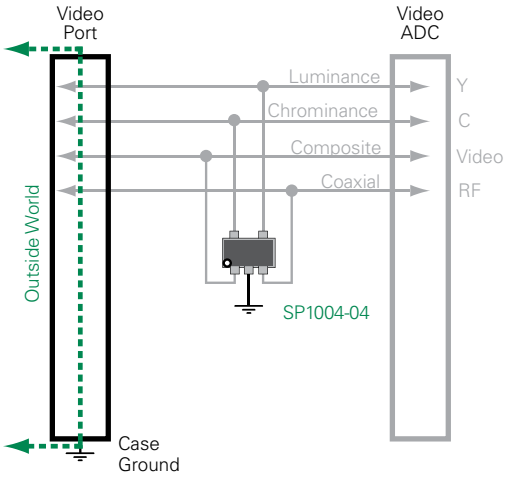
The following are examples of ESD suppression for ports common to entertainment electronics. For additional design examples, guidance and application assistance, please contact Littelfuse.

High Definition Multimedia Inteface (HDMI)

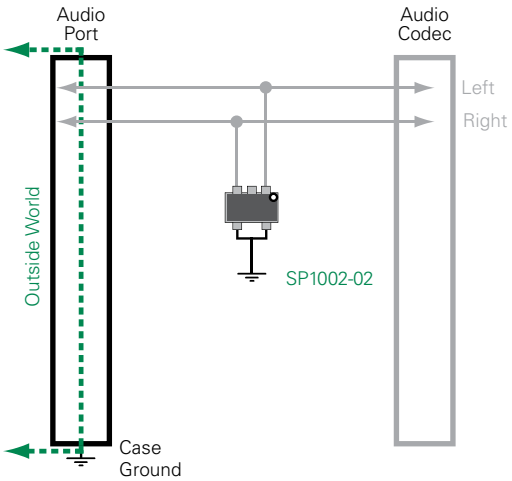
Data speeds up to 3.4 Gbps per pair



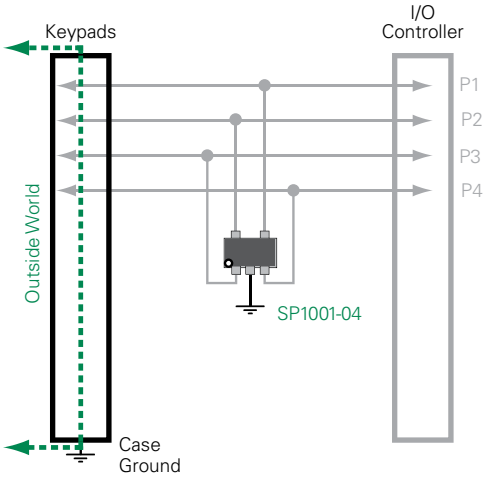
Analog Video Port



Analog audio (Speaker/Microphone)



Keypad / push button ESD protection



For additional reference design examples, please view the product data sheets within this catalog or visit the application reference design section of our web site http://www.littelfuse.com/design/application-design-center.html

To assure suitability of any Littelfuse device, be sure to test the device within the end application under conditions of intended use.

DEFINITIONS AND TERMS

Definitions

Operating Voltage Range (Vsupply)

The range limits of the power supply voltage that may be across the V+ and V- terminals. The SCR/Diode arrays do not have a fixed breakover or operating voltage. These devices 'float' between the input and power supply rails and thus the same device can operate at any potential within its range.

Forward Voltage Drop

The maximum forward voltage drop between an input pin and respective power supply pin for a specific forward current.

Reverse Voltage Drop

The maximum reverse voltage drop between an input pin and respective power supply pin for a specific reverse current.

Reverse Standoff Voltage

The device VR should be equal to, or greater than the peak operating level of circuit (or part of the circuit) to be protected. This is to ensure that SPA devices do not clip the circuit drive voltage.

Reverse Leakage Current

Maximum of state current measured at specified voltage.

Clamp Voltage

Maximum voltage which can be measured across the protector when subjected to the maximum peak pulse current. The "I_{PP}" or Peak Pulse Current is typically an 8x20µs waveform that aims to reduce voltage spikes due or overshoots due to parasitic PCB inductance.

Input Leakage Current

The DC current that is measured at the input pins at the stated voltage supplied to the input.

Quiescent Supply Current

The maximum DC current into V+/V- pins with Vsupply at its maximum voltage

Input Capacitance

The capacitance measured between the input pin and a reference (usually GND) with a 1MHz, 30 mV_{RMS} signal.

Liability

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TRANSIENT VOLTAGE THREATS AND SCENARIOS

Transient Threats – What Are Transients?

Voltage Transients are defined as short duration surges of electrical energy and are the result of the sudden release of energy previously stored or induced by other means, such as heavy inductive loads or lightning. In electrical or electronic circuits, this energy can be released in a predictable manner via controlled switching actions, or randomly induced into a circuit from external sources.

Repeatable transients are frequently caused by the operation of motors, generators, or the switching of reactive circuit components. Random transients, on the other hand, are often caused by Lightning and Electrostatic Discharge (ESD). Lightning and ESD generally occur unpredictably, and may require elaborate monitoring to be accurately measured, especially if induced at the circuit board level. Numerous electronics standards groups have analyzed transient voltage occurrences using accepted monitoring or testing methods. The key characteristics of several transients are shown in the table below.

	VOLTAGE	CURRENT	RISE-TIME	DURATION
Lighting	25kV	20kA	10 µs	1ms
Switching	600V	500A	50µs	500ms
EMP	1kV	10A	20ns	1ms
ESD	8kV	30A	<1ns	100ns

Table 1. Examples of transient sources and magnitude

Characteristics of Transient Voltage Spikes

Transient voltage spikes generally exhibit a "double exponential" wave, as shown below for lightning and ESD.

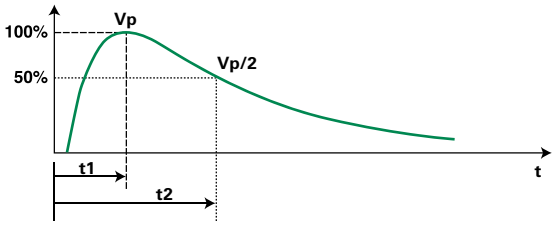


Figure 1. Lightning Transient Waveform

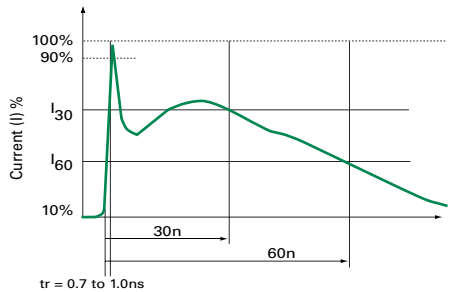


Figure 2. ESD Test Waveform

The exponential rise time of lightning is in the range 1.2µsec to 10µsec (essentially 10% to 90%) and the duration is in the range of 50µsec to 1000µsec (50% of peak values). ESD on the other hand, is a much shorter duration event. The rise time has been characterized at less than 1.0ns. The overall duration is approximately 100ns.

Why are Transients of Increasing Concern?

Component miniaturization has resulted in increased sensitivity to electrical stresses. Microprocessors for example, have structures and conductive paths which are unable to handle high currents from ESD transients. Such components operate at very low voltages, so voltage disturbances must be controlled to prevent device interruption and latent or catastrophic failures.

Sensitive microprocessors are prevelant today in a wide range of devices. Everything from home appliances, such as dishwashers, to industrial controls and even toys use microprocessors to improve functionality and efficiency.

Most vehicles now also employ multiple electronic systems to control the engine, climate, braking and, in some cases, steering, traction and safety systems.

Many of the sub- or supporting components (such as electric motors or accessories) within appliances and automobiles present transient threats to the entire system.

Careful circuit design should factor environmental scenarios as well as the potential effects of these related components. Table 2 below shows the typical vulnerability of various component technologies.

Device Type	Vulnerability (volts)
VMOS	30-1800
MOSFET	100-200
GaAsFET	100-300
EPROM	100
JFET	140-7000
CMOS	250-3000
Schottky Diodes	300-2500
Bipolar Transistors	380-7000
SCR	680-1000

Table 2: Range of device vulnerability (typical).

Electrostatic Discharge (ESD)

Electrostatic discharge is characterized by very fast rise times and very high peak voltages and currents. This energy is the result of an imbalance of positive and negative charges between objects.

ESD that is generated by everyday activities can far surpass the vulnerability threshold of standard semiconductor technologies. Following are a few examples:

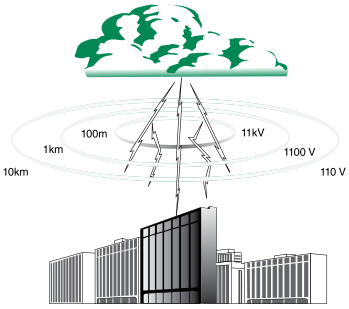
- **Walking across a carpet:**
  35kV @ RH = 20%;1.5kV @ RH = 65%
- **Walking across a vinyl floor:**
  12kV @ RH = 20%;250V @ RH = 65%
- **Worker at a bench:**
  6kV @ RH = 20%;100V @ RH = 65%
- **Vinyl envelopes:**
  7kV @ RH = 20%;600V @ RH = 65%
- **Poly bag picked up from desk:**
  20kV @ RH = 20%;1.2kV @ RH = 65%

Lightning In duced Transients

Even though a direct strike is clearly destructive, transients induced by lightning are not the result of a direct strike.

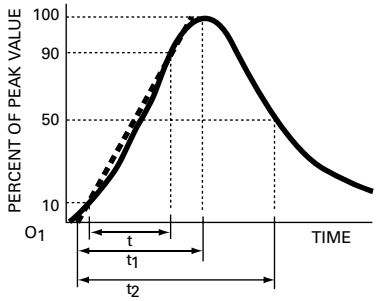
When a lightning strike occurs, the event creates a magnetic field which can induce transients of large magnitude in nearby electrical cables.

A cloud-to-cloud strike will effect not only overhead cables, but also buried cables. Even a strike 1 mile distant (1.6km) can generate 70 volts in electrical cables.



In a cloud-to-ground strike (as shown at right) the transient-generating effect is far greater.

This diagram shows a typical current waveform for induced lightning disturbances.



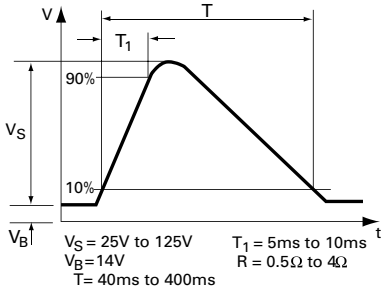
Inductive Load Switching

The switching of inductive loads generates high energy transients which increase in magnitude with increasingly heavy loads. When the inductive load is switched off, the collapsing magnetic field is converted into electrical energy which takes the form of a double exponential transient. Depending on the source, these transients can be as large as hundreds of volts and hundreds of Amps, with duration times of 400 milliseconds.

Typical sources of inductive transients include:

- **Generator**
- **Motor**
- **Relay**
- **Transformer**

These examples are common in electrical and electronic systems. Because the sizes of the loads vary according to the application, the wave shape, duration, peak current and peak voltage are all variables which exist in real world transients. Once these variables can be approximated, a suitable suppressor technology can be selected.



The diagram at right shows a transient which is the result of stored energy within the alternator of an automobile charging system.

A similar transient can also be caused by other DC motors in a vehicle. For example, DC motors power amenities such as power locks, seats and windows. These various applications of a DC motor can produce transients that are just as harmful to the sensitive electronic components as transients created in the external environment.

ESD SUPPRESSION STRATEGIES AND STANDARDS

Why Implement Circuit Protection?

It is important to consider that most electronic equipment will spend 99% of its useful life in environments where it is subject to ESD.

ESD can be generated from a wide range of everyday factors such as very dry air, static from plastics, or walking across a floor or carpet, and can be present during every phase of useful life from manufacturing, to product shipping, receiving, to field handling.

Electrostatic Discharge (ESD) causes millions of dollars worth of damage to electrical components, rendering circuit boards non-functional, and corrupting or erasing vital data. Often the damage is not detectable until a malfunction occurs. That could take weeks, months, or even years before an unpredictable and premature breakdown causes a field failure.

If you use electronic components or boards in your products, adding devices that suppress ESD damage can result in preventing damage to your company reputation and bottom line. Other tangible benefits include:

- Higher manufacturing yields
- Less rework and inventory
- Reduced overall costs
- Fewer field failures and warranty calls
- Increased product reliability
- More repeat business

Companies can also face legal liabilities if the product fails due to ESD/Transient damage. So it is important to include ESD/Transient Immunity in all phases of the project.

It is wise to factor Electrostatic Discharge (ESD) Immunity strategies early in design processes. If a device in development fails ESD immunity tests–the scramble to avoid complete redesign often leads to higher parts cost and more manual assembly during manufacturing.

There is little time to fully analyze which components do and do not provide ESD immunity. Worse, under pressure, finding comprehensive information tailored to ESD immunity design is very difficult, leaving your product vulnerable to ESD/Transient damage.

Littelfuse associates can help you address these challenges, offering extensive application expertise and product testing capabilities. Please contact your local Littelfuse representative for assistance.

ESD Electrical Characteristics

ESD, in contrast to switching and surge transients, has a very short transition from zero to maximum current and voltage. The rise time of an ESD event is less than 1 nanosecond (1ns), while the other transients take longer than 1 microsecond (1µs) to reach their peaks.

The International Electrotechnical Commission (IEC) has developed a model of an ESD event for the user environment. The model defined in the IEC61000-4-2 standard is used for determining if systems (computers, networks, cell phones, set top boxes, etc.) are susceptible to ESD events. The test specification quantifies the methodology for introducing ESD into the system as well as the various voltage and current levels that define the ESD event.

Internal circuits or ICs have some level of ESD protection "on chip"; however, they are almost always much less than the typical ESD levels seen in the field. Furthermore, the internal ICs are commonly evaluated using a manufacturing environment test standard (MIL-STD-883, Method 3015) that generates voltages and current levels far below that of the IEC "system level" standard. The current levels can differ by more than 100 fold, and more about this is discussed on page 12 in the section titled "ESD Immunity Test Standards".

ESD Damage Risks

A transient discharged into an electronic system creates three general types of adverse effects:

1. Soft Failures/Data Corruption: can occur to a part of the data stream, or the system may latch up. This is a temporary problem and is solved by data correction (for data corruption) or by re-booting the system (for latch up).

2. Latent Defects: A component might be partially degraded, but able to function properly. Typically a latent defect may cause a system to fail prematurely.

3. Catastrophic Failures: An internal component is rendered inoperable, and cannot function properly. This is a permanent condition. In the case of **Junction Burnout**, a short circuit condition is created in a transistor of the circuit. The metallic interconnect (Trace Line) is "pulled through" one of the semiconductor layers (Alloy Spike) or one of the semi conducting junctions is directly short circuited (Junction Short). In **Oxide Punch-Through**, the metallic interconnect is "pulled through" the oxide layer to provide a short circuit on the signal line. In **Metallization Burnout**, the metallic interconnect is melted, much like a fuse. It creates an open circuit condition on the signal line.

The use of ESD circuit protection components like Littelfuse SPA™ devices will help you avoid such problems.

ESD Suppression and Circuit Design Considerations

Proper use of circuit protection helps to reduce ESD risks. Littelfuse SPA devices possess the speed, clamping voltage, and residual current levels that will protect today's sensitive semiconductors and electronic circuitry. Many SPA devices present an extremely low parasitic capacitance to prevent signal degradation in high-speed/ high bandwidth communications.

When selecting ESD suppressors, designers need to consider potential coupling paths that would allow ESD to enter the circuit. These weak points should be considered for SPA device protection, selected with characteristics appropriate for the component sensitivity, and the equipment and environment where it will be used.

Common ESD Entry Points

ESD quickly finds weak spot(s) and will sneak into devices using a wide range of potential coupling paths. Careful consideratation about potential weak points, and taking steps to seal off those paths and fortify the most vulnerable electronic components is vital. Below are ways an ESD pulse can enter an electronic device:

1. An initial electric field from an arc can capacitively couple over a large surface area. It can appear like a signal to high-impedance analog circuits and measure up to 4000 V/m

2. Current or charge from the arc can be injected and:

- Smash through insulating layers in the component and damage the gates of MOSFETs and CMOS devices
- Trigger a latch-up in CMOS devices
- Short circuit reverse and forward-biased PN junctions
- Melt bonding wires

3. A voltage pulse on conductors caused by current (V = L * dI/dt) whether from ground, power or signal wiring, can spread into every device that is linked

4. An intense magnetic field emitted from an ESD arc can have a frequency range of 1 to 500Mhz, which can inductively couple into every nearby wiring loop and be as high as 15 A/m

5. An electro-magnetic field generated by the arc's magnetic field can radiate and couple into long wires that act like receiving antennas

ESD Suppression Strategies

Chip Level ESD Protection

In the heart of the device is the integrated circuitry (IC) responsible for its processing and communication function.

Typically, trade-offs for the chip designer are ESD protection versus die space and the demand of smaller and faster chips-which require sub-micron processes and very fine line widths. As more ESD protection structures are incorporated into the chip, survivability increases. The choice is either less space available for functional circuitry or make the chip larger.

In today's market, "smaller and faster" is the goal, and ESD protection is sacraficed for more on-chip space to boost functionality and speed. Consequently, circuits will become more sensitive to ESD and other transients.

Input and output port connections allow the free flow of data – including transients. ESD can enter a port–or the disconnected end of the cable while connecting/ disconnecting cables. It will then travel through the connector to the PC board and propagate down the data lines toward the ICs.

Littelfuse offers ultral-small size SPA packages to provide maximum protection with a minimum of space. The suppressor devices are installed between the data line and the chassis ground (parallel connection) and shunt the ESD transient from the data line to the ground. Optimally, SPA devices should be the first thing a transient should encounter on the board.

NOTE: For high-speed signal pins, devices with extremely low capacitance levels should be used. Consult www.littelfuse.com for more detailed information on which products offer best protection for high-speed connectors.

Board Level ESD Protection

Especially critical in portable systems is the board layout. Parasitic inductance in the protection path can result in significant voltage overshoot, easily getting past the insulation barriers and damaging the the circuit. This is especially critical in the case of fast rise-time transients such as ESD or EFT. However, the need for board-level protection will vary from system to system.

Factors determining level of need:

- The board layout
- ESD capabilities of the IC
- Physical ability of ESD transients to get on the data lines

Empirical testing can also be done to help determine the system's susceptibility.

ESD SUPPRESSION STRATEGIES AND STANDARDS (CONT.)

ESD Prevention During and After Manufacturing

Manufacturers typically include structures stamped directly on the die to provide some ESD protection of the circuits through the manufacturing process. Production environments tightly control and take precautions to ensure that static electricity levels on personnel and equipment are minimized. For example, when handling parts or their containers, workers wear wrist straps, anti-static garments and work at grounded workstations. Various environmental controls (humidity/air ionization) are also implemented. Finally, by transporting products in special electrostatic shield packaging ensures safe arrival to the customer.

More powerful transients await as the product moves outside the controlled factory environment. Often designers and/or engineers will need to provide additional off-chip, board-level solutions to fill in the gaps.

Ultimately, hardware or board designers must add supplementary ESD devices to protect these sensitive chipsets from the high level ESD threats seen in the field.

Supplemental ESD Protection

When deciding on more ESD protection, the next step is to identify the appropriate suppressor. Consider the following specifications to make an appropriate selection:

- Capacitance
- Peak voltage and clamping level
- Leakage current
- System operating voltage
- Number of lines to be protected

Capacitance is becoming an extremely important criterion since the data rates at which electronic products are communicating continue to increase. As previously mentioned, the **Clamping Level** of the suppressor determines how much of the ESD transient is eliminated. A related value is the **Peak Voltage.** As the suppressor transitions from high to low resistance, a portion of the ESD wave front is transmitted before the clamping voltage is established. These are important factors for those IC's that do not have a substantial amount of on-chip ESD protection. In this case, it is important that as little ESD as possible is actually experienced by the IC. For these circuits, Littelfuse Silicon Protection Arrays (SPA™) are ideal. They have extremely low peak and clamping voltages to provide ultimate protection to the IC.

Leakage Current is the amount of current passed through the suppressor as the circuit operates normally (i.e. at rated voltage). It is an important consideration for applications where the main power supply is battery-driven. In these cases, the suppressor should allow as little leakage as possible, to avoid increasing the battery drainage time.

All Littelfuse ESD suppressors have very low typical leakage current. Suppressors have varied **System Operating Voltage** specifications determined by their construction. This is used to determine if the part is suitable for given circuit parameters. For example, a 5 VDC-rated part should not be used where the ESD reference is a 9 VDC bus. The excess voltage may cause degradation of the part or even catastrophic failure due to excessive heating caused by DC current flow.

Another consideration is the **Number Of Lines To Be Protected.** This is determined by the system's data protocol. For example, USB buses have two data lines, RS 485 uses two lines per differential pair, 10/100 BaseT Ethernet uses four lines, etc. In cases where multiple data lines will be protected, it may be desirable to use a multi-line suppressor to save board space and installation costs. Littelfuse suppressors are available in single and multiple line packages to offer a broad selection of high quality SPA™ devices to the circuit designer.

Suppressor Location

Place the suppressor as near the line that it is protecting as possible, and as close as possible to the point of ESD entry. ESD transients should hit the suppressor first on entry to the board. Because ESD is such a fast rise-time event, any distance between the protected line and the ESD suppressor will mean more transient voltage to the IC.

ESD Immunity Test Standards

To test their products, manufacturers may apply one of several methods using either the CDM (Charged Device Model), MM (Machine Model), and/or HBM (Human Body Model). MIL-STD-883 Method 3015 and IEC61000-4-2 are testing standards commonly applied:

MIL-STD-883 Method 3015

Historically, analog and digital designers have been required to have ESD protection "on-chip" to protect the IC during manufacturing. The most commonly used ESD standard in the manufacturing environment is the MIL-STD-883, Method 3015 and it's also referred to as the Human Body Model (HBM). This model discharges a 100pF capacitor through a 1500Ω resistor into the device under test. The table below points out the four test levels as defined in the standard.

HBM Level	Contact Discharge (kV)	Peak Current (A)
1	±0.5	0.33
2	±1	0.67
3	±2	1.33
4	±4	2.67

The maximum level required for a typical IC had been ±2kV up until 2007, but today that level has been drastically reduced to ±0.5kV. Obviously, this has helped chip designers save valuable silicon area for more functionality, but in turn, it has made the IC much more susceptible to damage from ESD.

IEC61000-4-2

Conversely, equipment manufacturers have traditionally used an ESD standard defined by the IEC (International Electrotechnical Commission) for system or application level testing. This model uses a 150pF capacitor which is discharged through a 330Ω resistor. The table below displays the four test levels as defined in the standard.

IEC Level	Contact Discharge (kV)	Peak Current (A)
1	±2	7.5
2	±4	15
3	±6	22.5
4	±8	30

Most all manufacturers require that their equipment pass Level 4, or ±8kV, as a minimum, however, some are looking for increased reliability and require that their devices pass a much higher level like ±15kV or ±30kV.

The system level ESD test defined by the IEC produces a substantial increase in peak current compared to the military standard. If an IC is rated for 0.5kV per the MIL-STD and the equipment manufacturer tests this same IC at 8kV per the IEC specification, the chip will see nearly a 100 fold increase in peak current (i.e. 0.33A vs. 30A)!

Additional Transient Immunity Considerations

Film Resistors

In-line film resistors between inputs and off-board connectors provide minimal transient protection and are often damaged themselves.

Component Quality

Active components play the biggest role towards ESD/Transient immunity. If using substitute and/or secondary source components, test and analyze them thoroughly. Though functionally equivalent, they may lack the ESD/Transient immunity of the preferred components.

Multi-Suppressor Combinations

ESD protection through use of SPA™ devices included in combination with other filters and transient suppressors is another strategy for inputs, outputs and power nets. See www.Littelfuse.com for more information.

Preventive Software Programming

The basic requirement of good software is to cleanly handle abnormal operations, no matter the cause.

Internal Moving Parts

Equipment with moving parts can become its own ESD/Transient generator. Printers and copiers are especially susceptible because they carry paper through paper rollers and use toner. In general, the problem areas include sliding parts, rolling parts, flexing parts, flowing liquids and airflow carrying particles or liquid droplets.

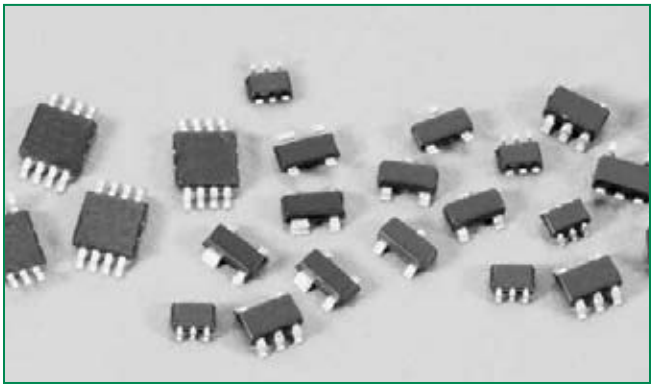
Finally, once the design has been approved, it's tempting to substitute components in effort to boost product performance. Often newer chips and components are faster but more sensitive to transients causing new emissions and immunity problems. Keep fully informed, as periodically suppliers can make changes to components that may affect ESD Immunity. Test the new parts to determine if they are still effective. Planning is key, in the event the new product doesn't work or the company ceases producing it, having several backup plans will help your company face unforseen challenges.

For More Information

Please visit www.littelfuse.com/esd for technical notes and application advice articles that address ways to reduce catastrophic failures and allow the equipment to reliably withstand certain ESD events.

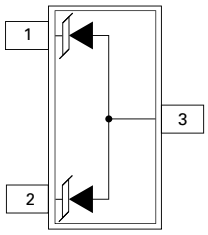
SP05 Series - 30pF 30kV Unidirectional TVS Array

HF RoHS GREEN

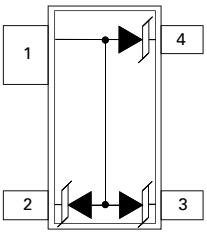


Pinout

SP0502BAHTG
SP0502BAJTG



SP0503BAHTG



SP0504BAHTG
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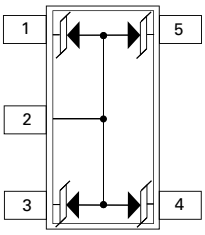

SP0505BAHTG
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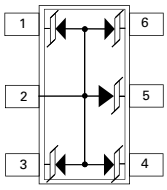
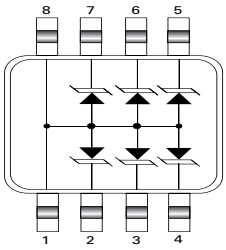


SP0506BAATG



Description

This surface mount family of arrays suppresses ESD and other transient overvoltage events. Used to meet the International Electrotechnical Compatibility (IEC transient immunity standards IEC 61000-4-2 for Electrostatic Discharge Requirements), these devices can help protect sensitive digital or analog input circuits on data, signal, or control lines with voltage levels up to 5VDC.

The monolithic silicon arrays are comprised of specially designed structures for transient voltage suppression (TVS). The size and shape of these structures have be tailored for transient protection. The low capacitance and clamp voltage are ideal for high speed signal line protection.

Features

- An Array of 2, 3, 4, 5 or 6 TVS Avalanche Diodes in a ultra small SC70, SOT-23, SOT-143 or MSOP packages
- ESD Capability Standards
  - IEC 61000-4-2, Direct Discharge ..... 30kV (Level 4)
  - IEC 61000-4-2, Air Discharge..... 30kV (Level 4)
  - MIL STD 883 3015.7.....30kV
- Input Protection for Applications Up to 5VDC
- Fast Response Time.....<1ns
- Low Input Capacitance.....30pF Typical
- Operating Temperature Range..... -40°C to 85°C

Applications

- Mobile phone handsets
- Personal Digital Assistants (PDA)
- Portable handheld equipment (Laptop, Palmtop computers)
- Computer port, keyboard (USB1.1)
- Digital still cameras
- Digital video cameras
- MP3 players

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

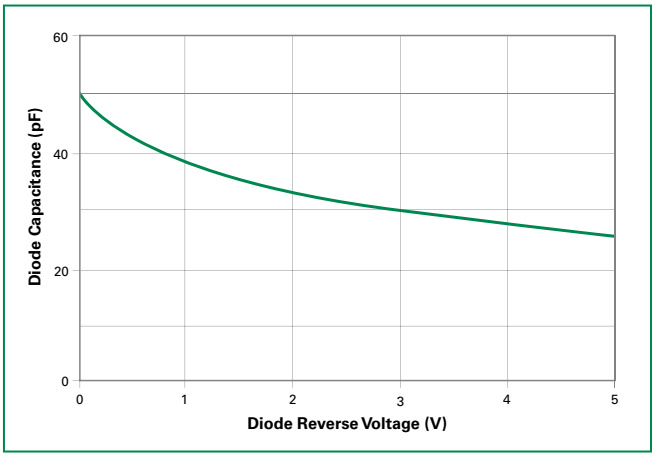
Parameter	Rating	Units
Storage Temperature Range	-65 to + 150	°C
Package Power Dissipation		
SC70	0.2	W
SOT23-3, SOT23-5, SOT23-6, SOT143	0.225	W
MSOP	0.5	W

Electrical Characteristics T_A = +25°C, Unless Otherwise Specified

Parameter	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	$I_R \leq 1\mu A$	-	-	5.5	V
Reverse Standoff Leakage Current	V = 5.0V		1	100	nA
Signal Clamp Voltage					
Positive	I = 1mA	7.0	7.8	8.5	V
Negative	I = 10mA	-1.2	-0.8	-0.4	V
Clamp Voltage during ESD					
MIL-STD-883 Method 3015 (HBM) test					
+ 8kV			12		V
- 8kV			-8		V
ESD Test Level (1)					
IEC-61000-4-2, Contact discharge		30			kV
MIL-STD-883 Method 3015 (HBM)		30			kV
Capacitance	2.5V @ 1MHz		30		pF
Turn on/off Time			<1		ns
Temperature Range					
Operating		-40		85	°C
Storage		-65		150	°C
Diode Dynamic Resistance					
Forward Conduction			1.0		Ω
Reverse Conduction			1.4		Ω

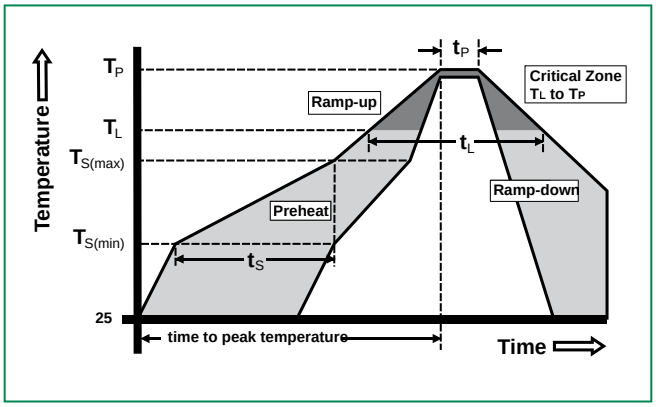
Note:
(1) ESD voltage applied between channel pins and ground, one pin at a time; all other channel pins are open; all ground pins are grounded.

Typical Diode Capacitance vs. Reverse Voltage

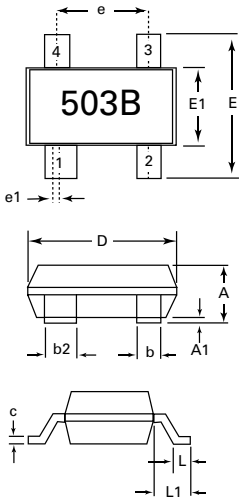


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

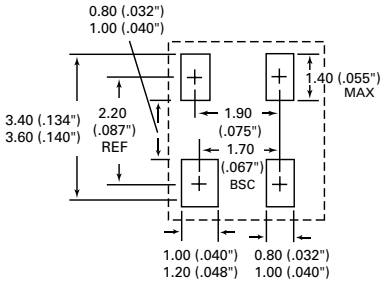


Package Dimensions — SOT143



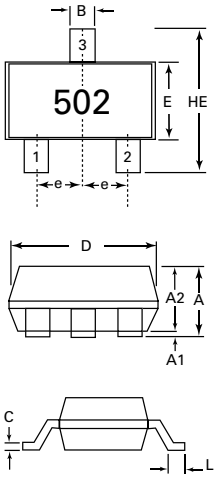
SP0503BAHTG - SOT143-4

Recommended Pad Layout



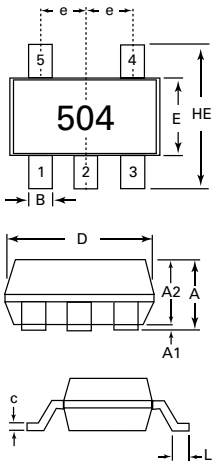
Package	SOT143-4			
Pins	4			
JEDEC	TO-253			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.8	1.22	0.03	0.048
A1	0.05	0.15	0.002	0.006
b	0.30	0.50	0.012	0.020
b2	0.76	0.89	0.030	0.035
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.082	0.104
E1	1.20	1.40	0.047	0.055
e	1.92 BSC		0.076 BSC	
e1	0.20 BSC		0.008 BSC	
L	0.4	0.6	0.016	0.024
L1	0.550 REF		0.022 REF	

Package Dimensions — SC70



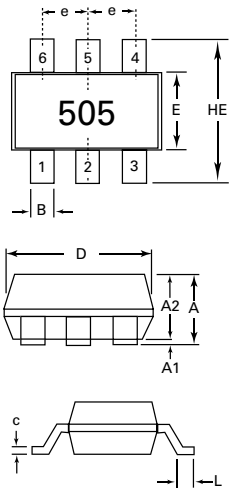
SP0502BAJTG - SC70-3

Package	SC70-3			
Pins	3			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.00	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.66 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018



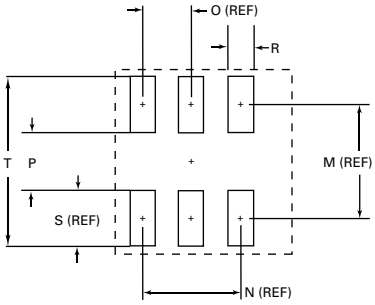
SP0504BAJTG - SC70-5

Package	SC70-5			
Pins	5			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.00	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018



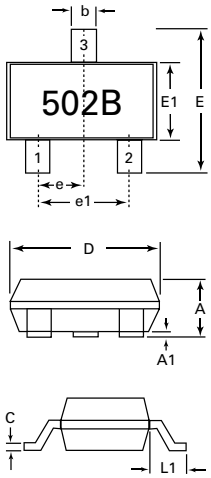
SP0505BAJTG - SC70-6

Recommended Pad Layout



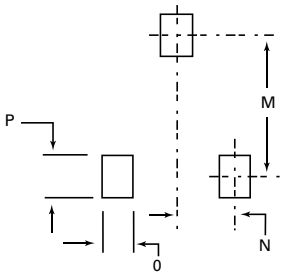
Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.00	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018
M	-	1.60	-	0.063
N	-	1.30	-	0.051
O	-	0.65	-	0.026
P	-	0.70	-	0.028
R	-	0.35	-	0.014
S	-	0.90	-	0.035
T	-	2.50	-	0.098

Package Dimensions — SOT23

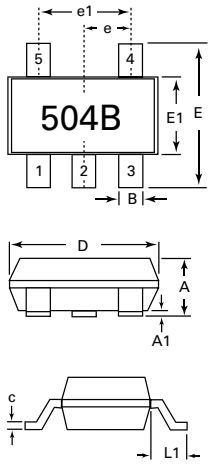


SP0502BAHT - SOT23-3

Recommended Pad Layout

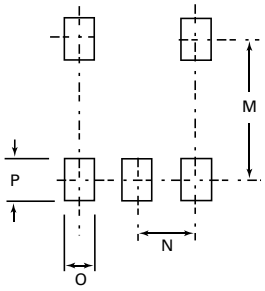


Package	SOT23-3			
Pins	3			
JEDEC	TO-236			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A1	0.01	0.1	0.0004	0.004
b	0.3	0.5	0.012	0.020
c	0.08	0.2	0.003	0.008
D	2.8	3.04	0.110	0.120
E	2.1	2.64	0.083	0.104
E1	1.2	1.4	0.047	0.055
e	0.95 BSC		0.038 BSC	
e1	1.90 BSC		0.075 BSC	
L1	0.54 REF		0.021 REF	
M		2.29		.090
N		0.95		0.038
O		0.78		.030TYP
P		0.78		.030TYP

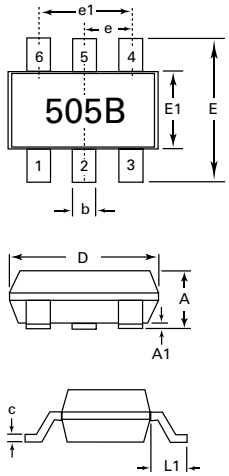


SP0504BAHTG - SOT23-5

Recommended Pad Layout

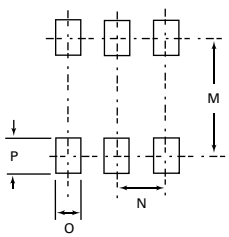


Package	SOT23-5			
Pins	5			
JEDEC	MO-178			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.45	-	0.057
A1	0	0.15	0	0.006
b	0.3	0.5	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.75	3.05	0.108	0.120
E	2.6	3.0	0.102	0.118
E1	1.45	1.75	0.057	0.069
e	0.95 BSC		0.038 BSC	
e1	1.90 BSC		0.075 BSC	
L1	0.60 REF		0.024 REF	
M		2.59		.102
N		0.95		.038
O		0.69		.027TYP
P		0.99		.039TYP



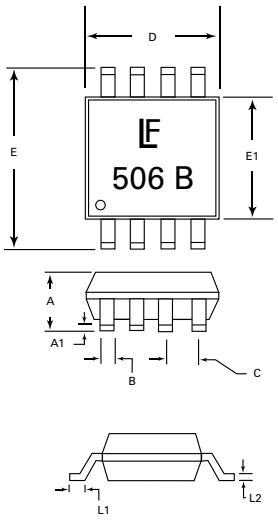
SP0505BAHTG - SOT23-6

Recommended Pad Layout



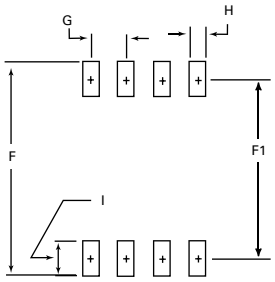
Package	SOT23-6			
Pins	6			
JEDEC	MO-178			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.45	-	0.057
A1	0	0.15	0	0.006
b	0.3	0.5	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.75	3.05	0.108	0.120
E	2.6	3.0	0.102	0.118
E1	1.45	1.75	0.057	0.069
e	0.95 BSC		0.038 BSC	
e1	1.90 BSC		0.075 BSC	
L1	0.60 REF		0.024 REF	
M		2.59		.102
N		0.95		0.038
O		0.69		.027TYP
P		0.99		.039TYP

Package Dimensions — MSOP



SP0506BAATG - MSOP-8

Recommended Pad Layout



Package	MSOP-8			
Pins	8			
	Millimeters		Inches	
	Min	Max	Min	Max
D	2.90	3.10	0.114	.122
E	4.78	4.98	.188	.196
E1	2.90	3.10	.114	.122
A	0.87	1.17	.034	.046
A1	0.05	0.25	.002	0.010
B	-	0.30TYP	-	0.012TYP
C	-	0.65TYP	-	0.026TYP
L1	0.52	0.54	0.020	0.021
L2	-	0.18TYP	-	.007TYP
F	-	5.28	-	.208
F1	-	4.24	-	.167
G	-	0.65	-	0.026
H	-	0.38	-	.015
I	-	1.04	-	.041

Part Numbering System

SP0502BAHTG

- SP: Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- 05: Series
- 02: Number of Channels
  - 02 = 2 channel (SC70-3, SOT23 packages)
  - 03 = 3 channel (SOT143 package)
  - 04 = 4 channel (SC70-5, SOT23-5 package)
  - 05 = 5 channel (SC70-6, SOT23-6 packages)
  - 06 = 6 channel (MSOP-8 package)
- BA: Package
  - BAA = MSOP-8
  - BAH = SOT23-3, -5, -6 or SOT143-4
  - BAJ = SC70-3, -5 or -6
- T: T= Tape & Reel
- G: Blank = NOT Green/RoHS/Lead Free*, G= Green/RoHS/Lead Free Product

Product Characteristics

Lead Plating	"G" Green version - Matte Tin (Sn)
Lead Material	Copper / Iron Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes:

1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 ISSUE A.
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

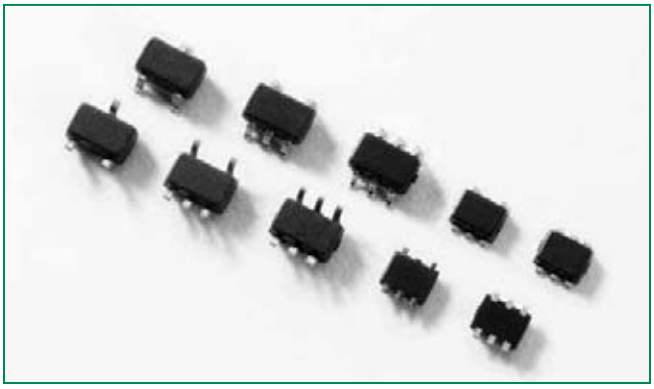
Ordering Information

*NOTE: To order NON-Green/RoHS/Lead Free version of product, remove "G" at the end of part number.

Part Number	CH	Package Type	Quantity Per Reel
SP0502BAHTG	2	SOT23-3	3000
SP0503BAHTG	3	SOT143-4	3000
SP0504BAHTG	4	SOT23-5	3000
SP0505BAHTG	5	SOT23-6	3000
SP0506BAATG	6	MSOP-8	4000
SP0502BAJTG	2	SC70-3	3000
SP0504BAJTG	4	SC70-5	3000
SP0505BAJTG	5	SC70-6	3000

SP1001 Series - 8pF 15kV Unidirectional TVS Array

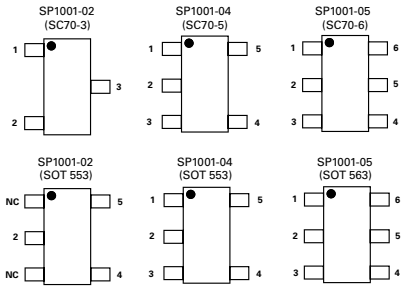
HF RoHS GREEN



Description

Zener diodes fabricated in a proprietary silicon avalanche technology protect each I/O pin to provide a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high-speed signal pins.

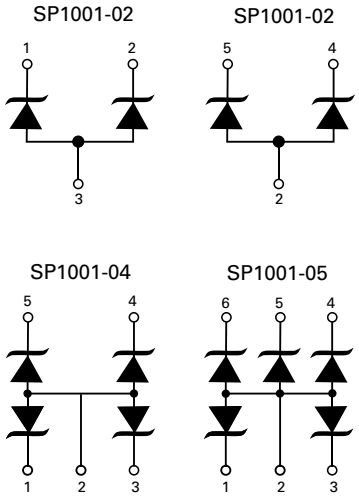
Pinout



Features

- Low capacitance of 8pF (TYP) per I/O
- ESD protection of ±15kV contact discharge, ±30kV air discharge, (Level 4, IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small package saves board space
- Lightning Protection, IEC61000-4-5, 2A (8/20µs)

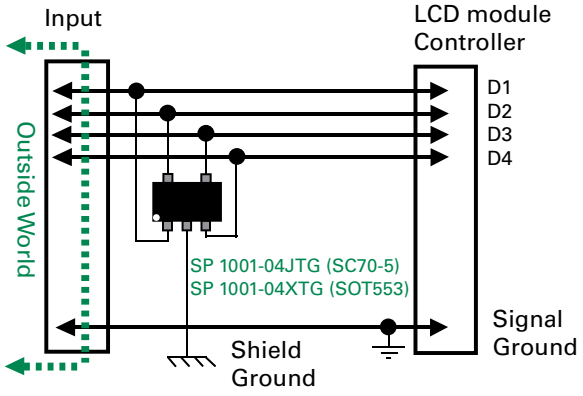
Functional Block Diagram



Applications

- Computer Peripherals
- Mobile Phones
- Digital Cameras
- Desktops/Notebooks
- LCD/PDP TVs
- Set Top Boxes
- DVD Players
- MP3/PMP

Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	2	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20s-40s)	260	°C

Electrical Characteristics (T_{OP} = 25°C)

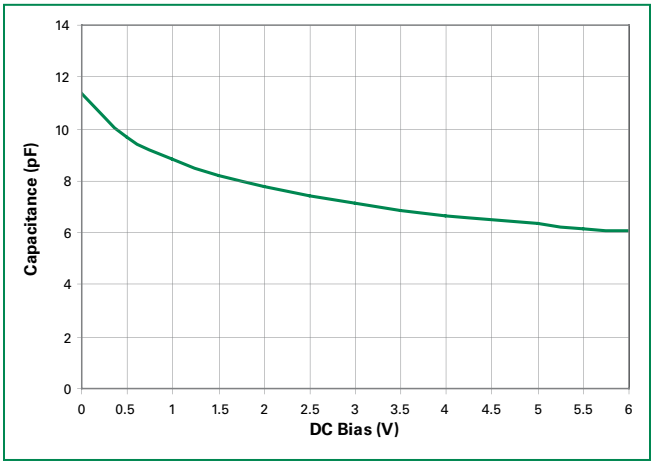
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Forward Voltage Drop	V_F	I_F=10mA	0.7	0.9	1.2	V
Reverse Voltage Drop	V_R	I_R=1mA	7.0	7.8	8.5	V
Reverse Standoff Voltage	V_{RWM}	I_R≤1µA			5.5	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		8.0	11.0	V
		I_{PP}=2A, t_p=8/20µs, Fwd		9.7	13.0	V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		1.7		Ω
ESD Withstand Voltage[1,2]	V_{ESD}	IEC61000-4-2 (Contact)	±15			kV
		IEC61000-4-2 (Air)	±30			kV
Diode Capacitance[1]	C_D	Reverse Bias=0V		12		pF
		Reverse Bias=2.5V		8		pF
		Reverse Bias=5V		7		pF

Notes:

[1] Parameter is guaranteed by device characterization

[2] A minimum of 1,000 ESD pulses are applied at 1s intervals between the anode and common cathode of each diode

Capacitance vs. Reverse Bias

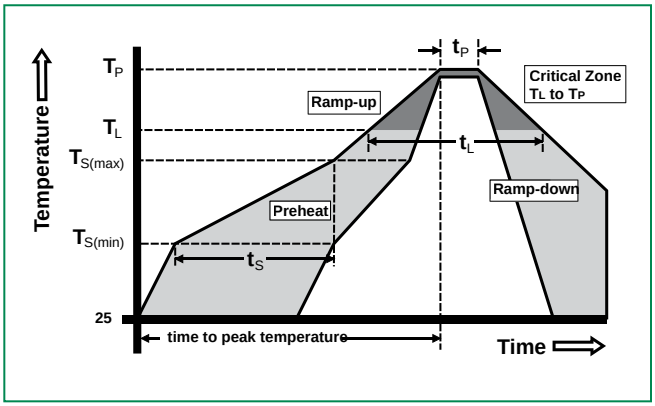


Design Consideration

Because of the fast rise-time of the ESD transient, placement of ESD devices is a key design consideration. To achieve optimal ESD suppression, the devices should be placed on the circuit board as close to the source of the ESD transient as possible. Install the ESD suppressors directly behind the connector so that they are the first board-level circuit component encountered by the ESD transient. They are connected from signal/data line to ground.

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes max.
Do not exceed		260°C

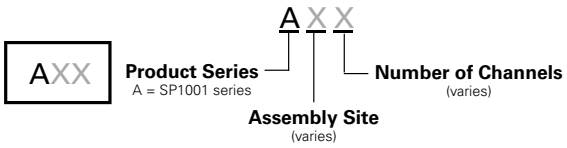


Part Numbering System

SP1001-02 J T G

- Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- Series
- Number of Channels
  - 02 = 2 Channel
  - 04 = 4 Channel
  - 05 = 5 Channel
- Package
  - J = SC70-3, -5 or -6, 3000 qty
  - X = SOT553 or SOT563, 5000 qty
- T= Tape & Reel
- G= Green

Part Marking System



Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP1001-02JTG	SC70-3	AX2	3000
SP1001-02XTG	SOT553	AX2	5000
SP1001-04JTG	SC70-5	AX4	3000
SP1001-04XTG	SOT553	AX4	5000
SP1001-05JTG	SC70-6	AX5	3000
SP1001-05XTG	SOT563	AX5	5000

Product Characteristics

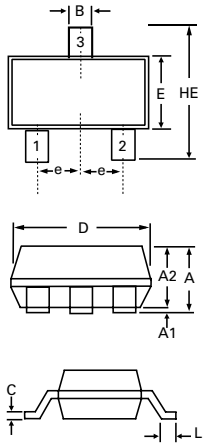
Lead Plating	Matte Tin (SC70-x) Pre-Plated Frame (SOT5x3)
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :

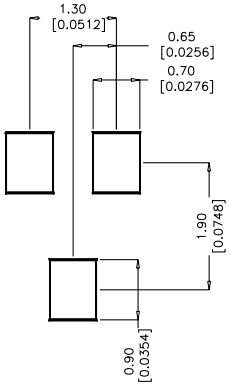
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Package Dimensions — SC70

SC70-3

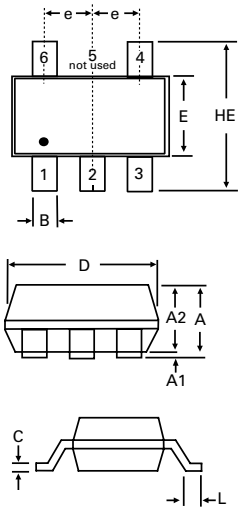


Solder Pad Layout

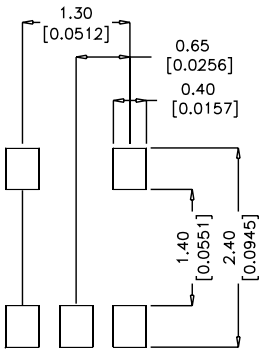


Package	SC70-3			
Pins	3			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.66 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

SC70-5

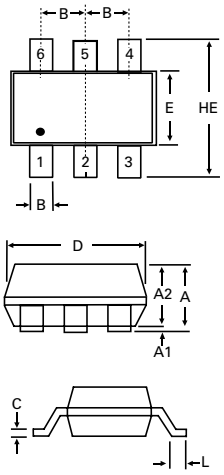


Solder Pad Layout

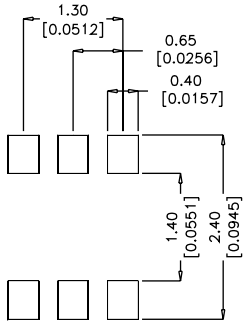


Package	SC70-5			
Pins	5			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

SC70-6

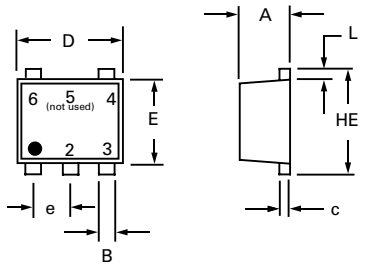


Solder Pad Layout



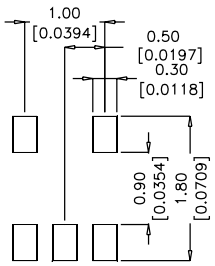
Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions — SOT5

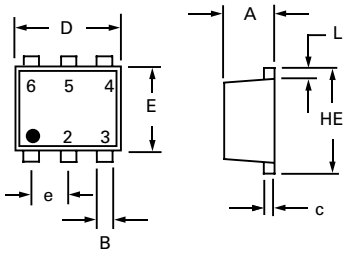


SOT 553

Solder Pad Layout

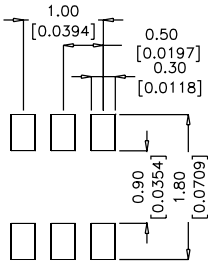


Package	SOT 553			
Pins	5			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067



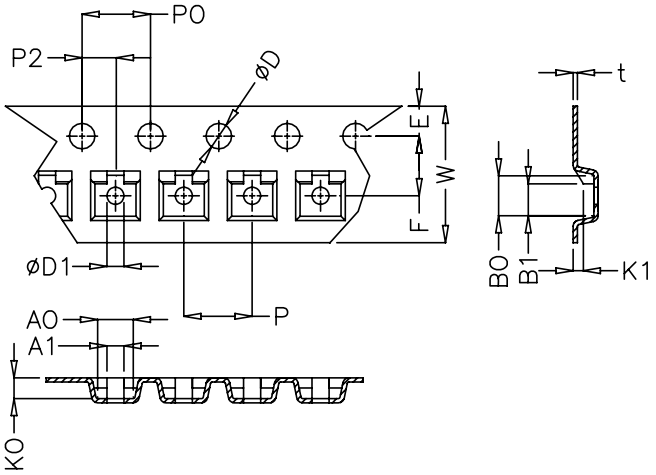
SOT 563

Solder Pad Layout



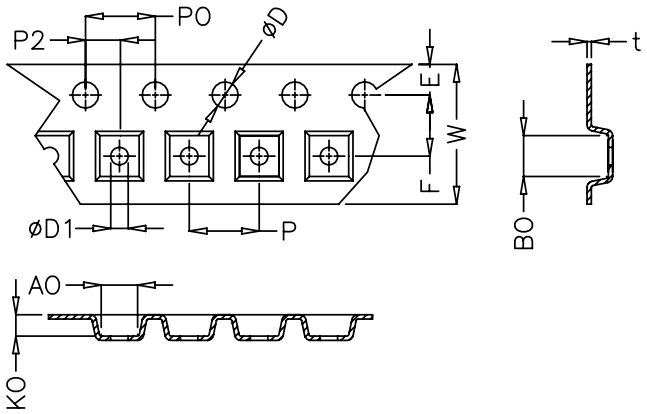
Package	SOT 563			
Pins	6			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

Embossed Carrier Tape & Reel Specification — SC70-3



Dimensions				
	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.30	2.50	0.090	0.098
A1	1.00 Ref		0.039 Ref	
B0	2.30	2.50	0.090	0.098
B1	1.90 Ref		0.074	
K0	1.10	1.30	0.043	0.051
K1	0.60 Ref		0.023 Ref	
t	0.27 max		0.010	

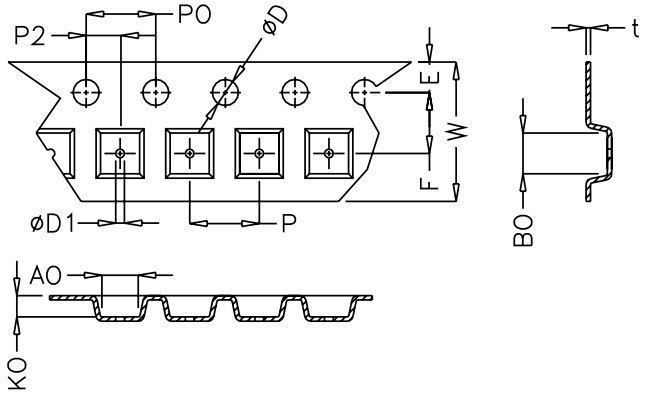
Embossed Carrier Tape & Reel Specification — SC70-5 and SC70-6



Dimensions

	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.096
K0	1.12	1.32	0.044	0.052
t	0.27 max		0.010 max	

Embossed Carrier Tape & Reel Specification — SOT553 and SOT563

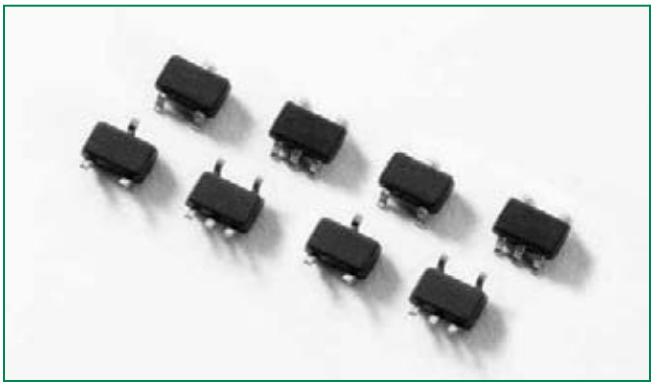


Dimensions

	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	0.45	0.55	0.017	0.021
P0	3.90	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	1.73	1.83	0.068	0.072
B0	1.73	1.83	0.068	0.072
K0	0.64	0.74	0.025	0.029
t	0.22 max		.009 max	

SP1002 Series 5pF 8kV Bidirectional TVS Array

HF RoHS GREEN

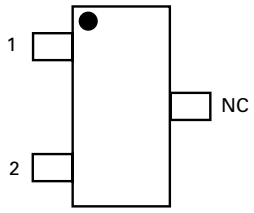


Description

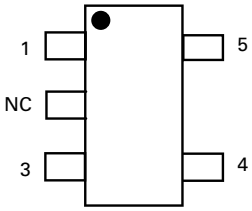
Back-to-Back Zener diodes fabricated in a proprietary silicon avalanche technology protect each I/O pin to provide a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high-speed signal pins.

Pinout

SP1002-01JTG
(SC70-3)



SP1002-02JTG
(SC70-5)

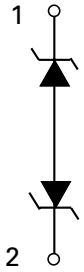


Features

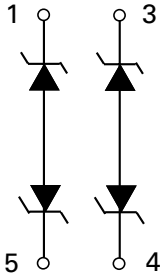
- Low capacitance of 5pF (TYP) I/O to I/O
- ESD protection of ±8kV contact discharge, ±15kV air discharge, (Level 4, IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small package saves board space
- Lightning Protection, IEC61000-4-5, 2A (8/20µs)

Functional Block Diagram

SP1002-01JTG



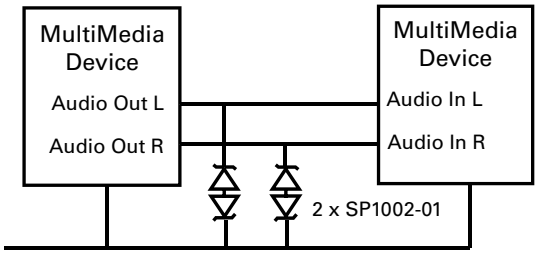
SP1002-02JTG



Applications

- Computer Peripherals
- Mobile Phones
- Digital Cameras
- Desktops/Notebooks
- LCD/PDP TVs
- Set Top Boxes
- DVD Players
- MP3/PMP

Application Example



SCART MultiMedia Application of SP1002-01

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20μs)	2	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

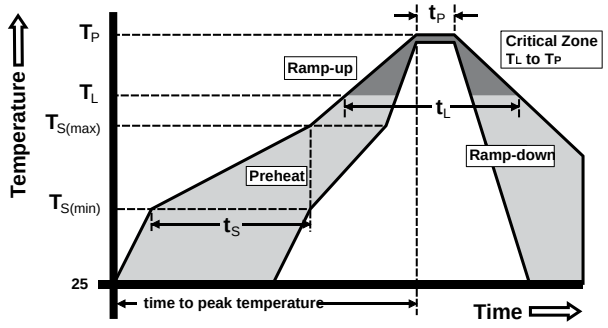
Electrical Characteristics (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Voltage Drop	V_D	I_R=1mA	8.0	8.8	9.5	V
Reverse Standoff Voltage	V_{RWM}	I_R≤1μA with 1 I/O at GND			6.0	V
Leakage Current	I_{LEAK}	V_R=5V with I/O at GND			0.5	μA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20μs, Fwd		9.2	13.0	V
		I_{PP}=2A, t_p=8/20μs, Fwd		11.2	16.0	V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		2.0		Ω
ESD Withstand Voltage[1,2]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	C_D	Reverse Bias=0V		6		pF
		Reverse Bias=2.5V		5		pF
		Reverse Bias=5V		5		pF

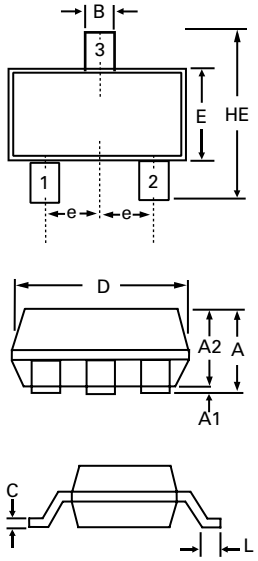
Notes:
[1] Parameter is guaranteed by device characterization
[2] A minimum of 1,000 ESD pulses are applied at 1s intervals

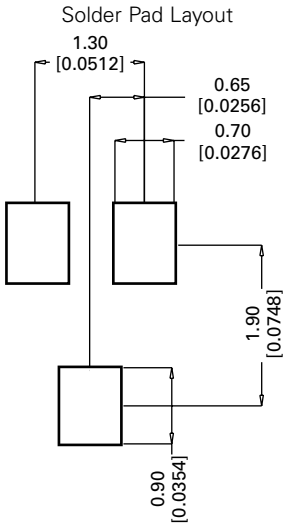
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes max.
Do not exceed		260°C



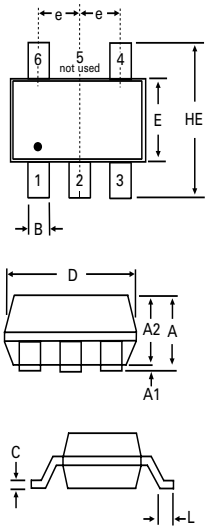
Package Dimensions — SC70-3

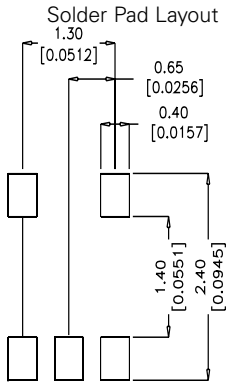




Package	SC70-3			
Pins	3			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.66 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions — SC70-5





Package	SC70-5			
Pins	5			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

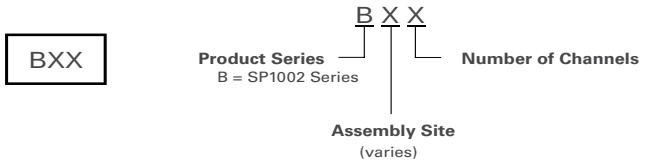
Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Part Numbering System

SP 1002 - XX J T G

- Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- Series
- Number of Channels
  - -01 = 1 Channel, SC70-3 Package
  - -02 = 2 Channel, SC70-5 Package
- Package
  - J = SC70-3
  - SC70-5
- T= Tape & Reel
- G= Green

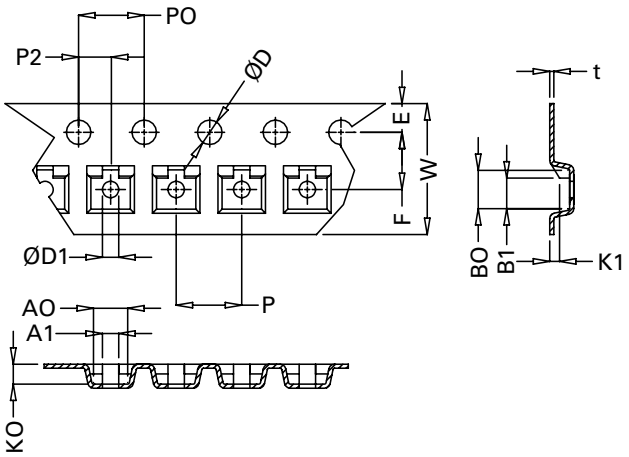
Part Marking System



Ordering Information

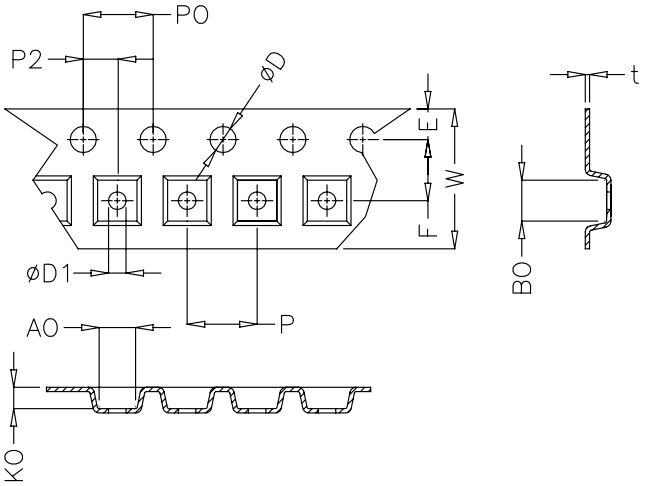
Part Number	Package	Marking	Min. Order Qty.
SP1002-01JTG	SC70-3	BX1	3000
SP1002-02JTG	SC70-5	BX2	3000

Embossed Carrier Tape & Reel Specification — SC70-3



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.30	2.50	0.090	0.098
A1	1.00 Ref		0.039 Ref	
B0	2.30	2.50	0.090	0.098
B1	1.90 Ref		0.074	
K0	1.10	1.30	0.043	0.051
K1	0.60 Ref		0.023 Ref	
t	0.27 max		0.010	

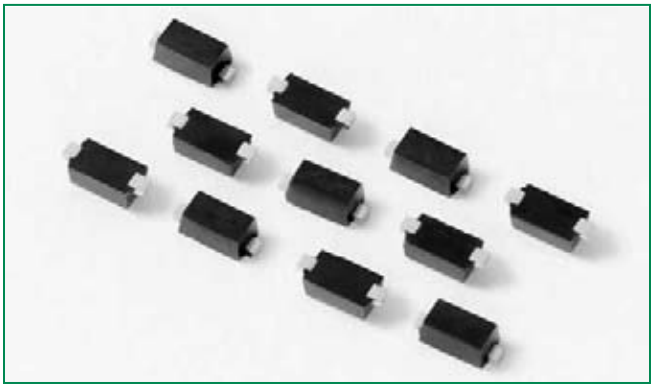
Embossed Carrier Tape & Reel Specification — SC70-5 and SC70-6



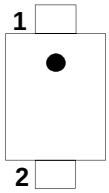
	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.096
K0	1.12	1.32	0.044	0.052
t	0.27 max		0.010 max	

SP1003 Series - 30pF 30kV Unidirectional Discrete TVS

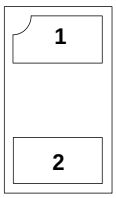
HF RoHS GREEN



Pinout

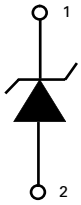


SOD723



SOD882

Functional Block Diagram



Description

Zener diodes fabricated in a proprietary silicon avalanche technology protect each I/O pin to provide a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at ±30kV (contact discharge, IEC 61000-4-2) without performance degradation. Additionally, each diode can safely dissipate 7A of 8/20µs surge current (IEC61000-4-5) with very low clamping voltages.

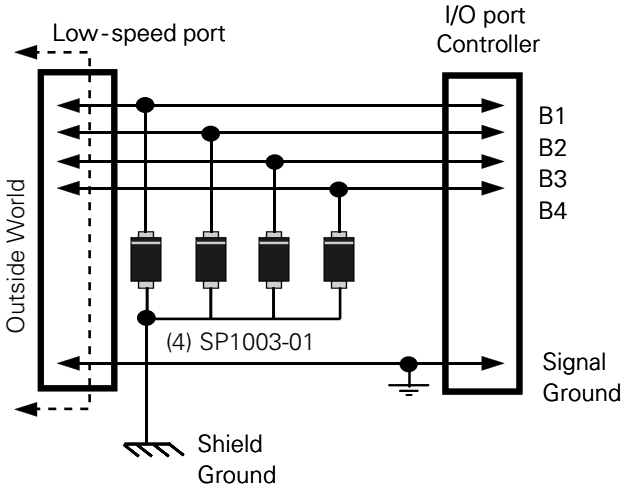
Features

- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 7A (8/20µs)
- Low leakage current of 100nA (MAX) at 5V
- Tiny SOD723/ SOD882 package saves board space
- Fits solder footprint of industry standard 0402 (1005) devices

Applications

- Mobile phones
- Smart phones
- PDAs
- Portable navigation devices
- Digital cameras
- Portable medical devices

Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current (t_p=8/20μs)	7.0	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

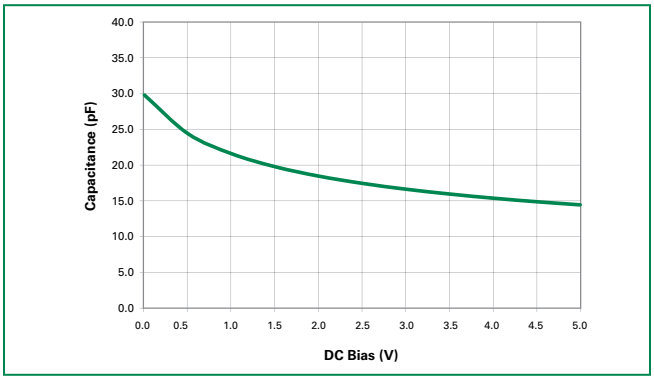
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

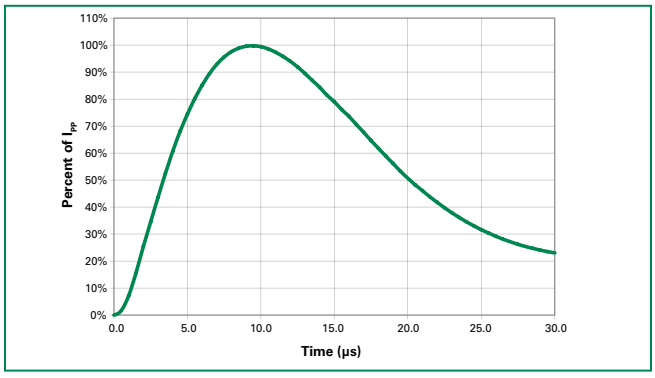
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Forward Voltage Drop	V_F	I_F = 10mA		0.8	1.2	V
Reverse Voltage Drop	V_R	I_R=1mA	7.0	7.8	8.5	V
Reverse Standoff Voltage	V_{RWM}	I_R≤1μA			5.0	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			100	nA
Clamp Voltage[1]	V_C	I_{pp}=6A t_p=8/20μs		11.4		V
		I_{pp}=7A t_p=8/20μs		12.0		V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		0.6		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact Discharge)	±30			kV
		IEC61000-4-2 (Air Discharge)	±30			kV
Diode Capacitance[1]	C_D	Reverse Bias=0V		30		pF

Note: [1] Parameter is guaranteed by design and/or device characterization.

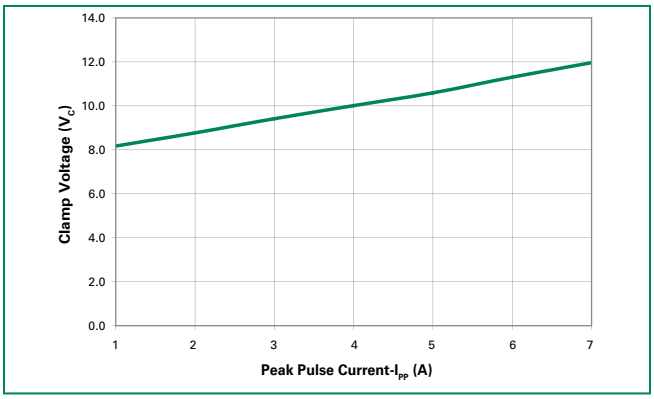
Capacitance vs. Reverse Bias



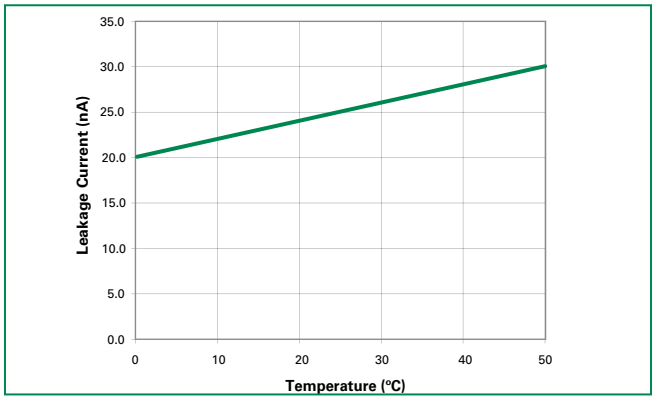
Pulse Waveform



Clamping Voltage vs. I_{PP}

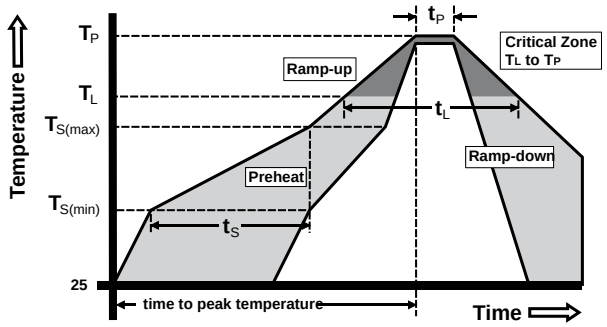


Leakage vs. Temperature

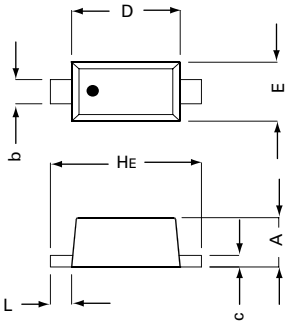


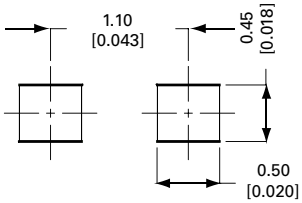
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — SOD723

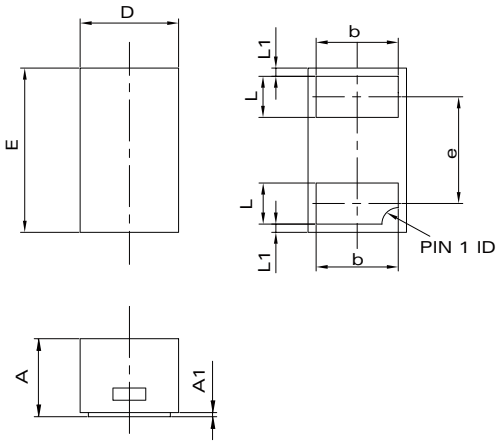




Recommended Solder Pad Layout
Millimeters (Inches)

Symbol	SOD723			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.46	0.65	0.018	0.026
b	0.23	0.35	0.009	0.014
c	0.08	0.13	0.003	0.005
D	0.90	1.10	0.035	0.043
E	0.58	0.64	0.023	0.025
HE	1.37	1.47	0.054	0.058
L	0.15	0.25	0.006	0.010

Package Dimensions — SOD882



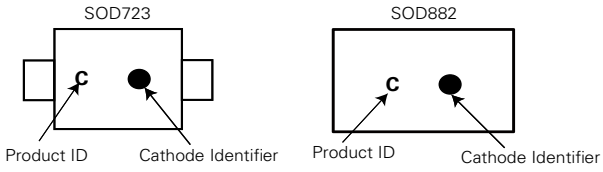
Symbol	SOD882			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.40	0.50	0.016	0.02
A1	0.00	0.05	0.000	0.002
D	0.55	0.65	0.022	0.026
E	0.95	1.05	0.037	0.041
b	0.40	0.60	0.016	0.024
e	0.65 TYP		0.026 TYP	
L	0.15	0.35	0.006	0.014
L1	0.05 REF		0.002 REF	

Part Numbering System

SP 1003 - 01 X T G

- SP: Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- 1003: Series
- 01: Number of Channels
- X: Package D: SOD723 E: SOD882
- T= Tape & Reel
- G= Green

Part Marking System



Product Characteristics

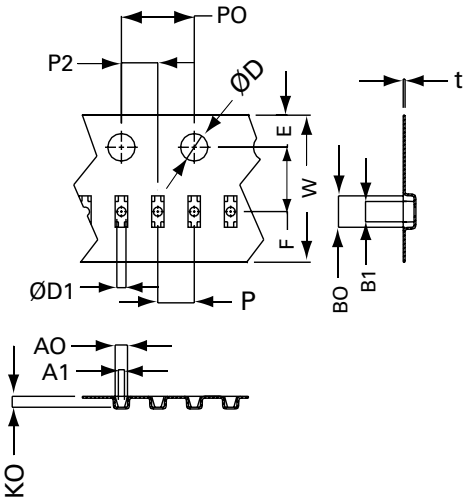
Lead Plating	Pre-Plated Frame or Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

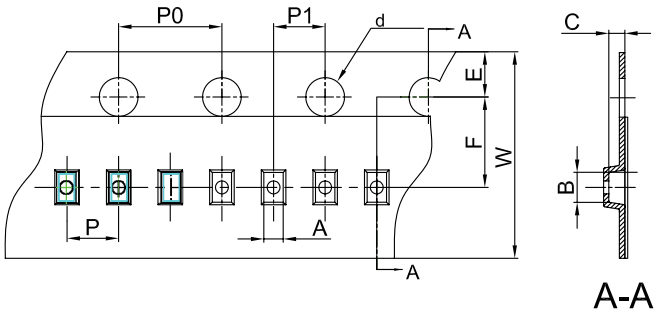
Part Number	Package	Marking	Min. Order Qty.
SP1003-01DTG	SOD723	C	8000
SP1003-01ETG	SOD882	C	8000

Embossed Carrier Tape & Reel Specification — SOD723



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.072
F	3.40	3.60	0.134	0.142
D1	0.45	0.55	0.017	0.021
D	1.50	- -	0.060	- -
PO	3.90	4.10	0.153	0.161
10PO	40.0+/- 0.20		1.570+/-0.010	
W	7.90	8.20	0.311	0.322
P2/P	1.90	2.10	0.074	0.082
AO	0.60	0.80	0.024	0.032
A1	0.33 REF		0.010 REF	
BO	1.61	1.81	0.063	0.071
B1	1.10 REF		0.040 REF	
KO	0.54	0.78	0.021	0.031
t	- -	0.21	- -	0.008

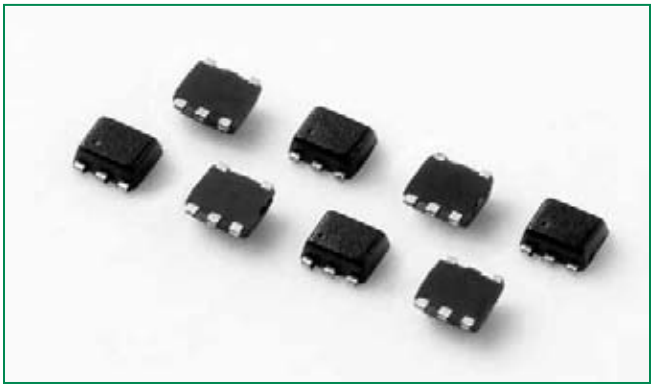
Embossed Carrier Tape & Reel Specification — SOD882



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
A	0.65	0.70	0.026	0.028
B	1.10	1.20	0.043	0.047
C	0.50	0.60	0.020	0.024
dØ	1.40	1.60	0.055	0.063
E	1.65	1.85	0.065	0.073
F	3.40	3.60	0.134	0.142
P0	3.90	4.10	0.154	0.161
P	1.90	2.10	0.075	0.083
P1	1.90	2.10	0.075	0.083
W	7.90	8.10	0.311	0.319

SP1004 Series 5pF 8kV Bidirectional TVS Array

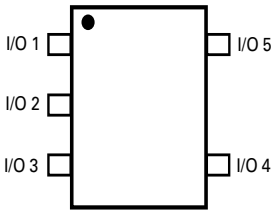
HF RoHS GREEN



Description

Back-to-back zener diodes fabricated in a proprietary silicon avalanche technology protect each I/O pin to provide a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high-speed signal pins.

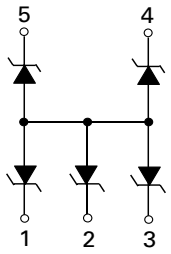
Pinout



SOT953

Notes:
[1]Any of the 5 I/O pins can be tied to GND to provide 4 channels of bidirectional protection

Functional Block Diagram



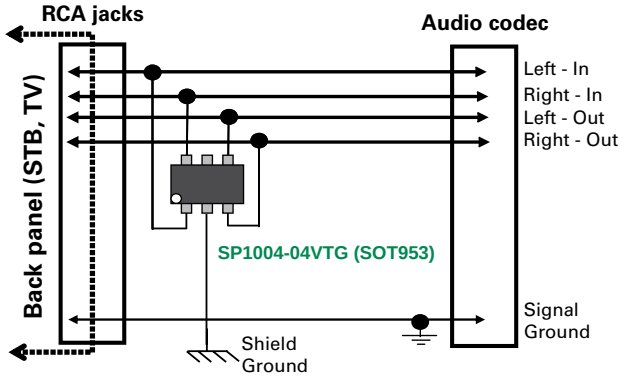
Features

- ESD, IEC61000-4-2, ±8kV contact, ±15kV air
- Capable of withstanding >1,000 ±8kV ESD strikes
- Lightning, IEC61000-4-5, 2A (t_p=8/20µs)
- Low capacitance of 5pF (TYP) per I/O
- Low leakage current of 1µA (MAX) at 5V
- Small SOT953 package

Applications

- MP3-PMPs
- DVD players
- Desktops
- Mobile phones
- Digital cameras
- Set top boxes
- Notebooks

Application Example



Life Support Note:
Not Intended for Use in Life Support or Life Saving Applications
The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current (t_p=8/20μs)	2.0	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

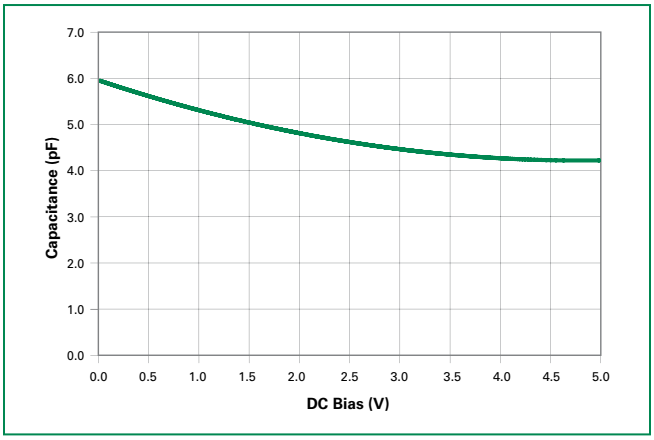
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

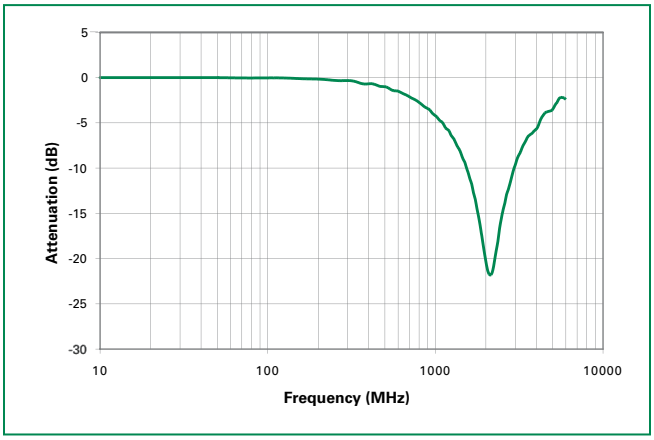
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Voltage Drop[1]	V_R	I_R=1mA	8.0	8.8	9.5	V
Reverse Standoff Voltage[1]	V_{RWM}	I_R≤1μA			6.0	V
Reverse Leakage Current[1]	I_{LEAK}	V_R=5V			0.1	μA
Clamp Voltage[2]	V_C	I_{PP}=1A, t_p=8/20μs		10		V
		I_{PP}=2A, t_p=8/20μs		12		V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		2.0		Ω
ESD Withstand Voltage[1,2]	V_{ESD}	IEC61000-4-2 (Contact Discharge)[3]	±8			kV
		IEC61000-4-2 (Air Discharge)	±15			kV
Diode Capacitance[1,2]	C_D	Reverse Bias=0V		6	7	pF
		Reverse Bias=1.5V		5	6	pF

Note: [1] Parameter specified with pin 2 grounded externally.
[2] Parameter is guaranteed by design and/or device characterization.
[3] Capable of withstanding >1,000 pulses at 1s intervals.

Capacitance vs. Reverse Bias

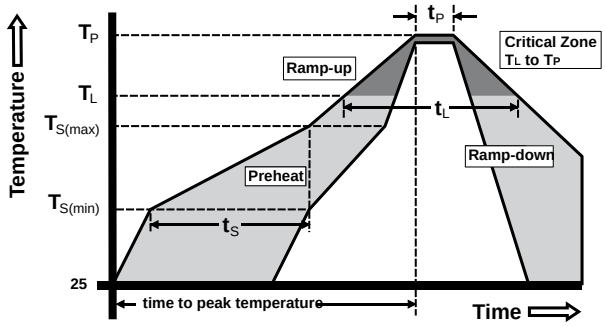


Insertion Loss (S21)

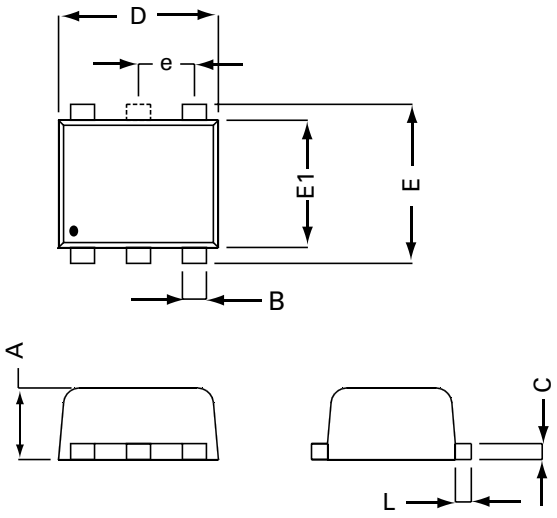


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

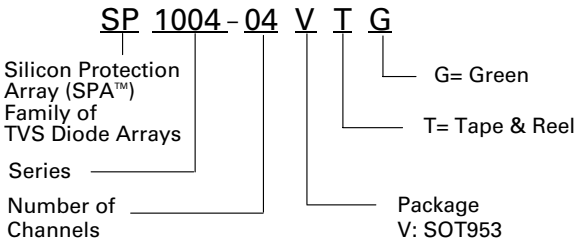


Package Dimensions — SOT953

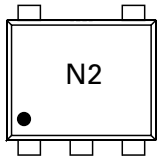


Symbol	SOT953			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.44	0.5	0.170	0.020
B	0.10	0.20	0.004	0.008
c	0.05	0.15	0.002	0.006
D	0.95	1.05	0.037	0.041
E	0.95	1.05	0.037	0.041
E1	0.75	0.85	0.029	0.033
e	0.35 BSC		0.014 BSC	
L	0.05	0.15	0.002	0.006

Part Numbering System



Part Marking System



Product Characteristics

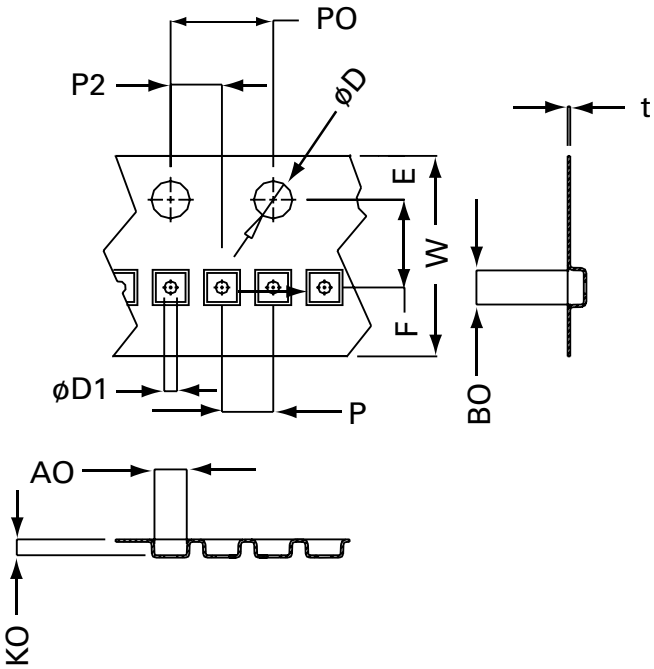
Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP1004-04VTG	SOT953	N2	8000

Embossed Carrier Tape & Reel Specification – SOT953



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.136	0.140
D1	0.45	0.55	0.018	0.022
D	1.50 min		0.059 min	
P0	3.90	4.10	0.154	0.161
10P0	40.0 +/- 0.20		1.575 +/- 0.008	
P	1.95	2.05	0.077	0.081
P2	1.95	2.05	0.077	0.081
W	7.90	8.20	0.311	0.323
A0	1.11	1.21	0.044	0.048
B0	1.11	1.21	0.044	0.048
K0	0.58	0.68	0.023	0.027
t	0.22 max		0.009 max	

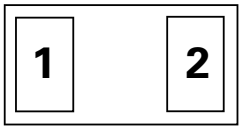
SP1005 Series 30pF 30kV Bidirectional Discrete TVS

HF RoHS GREEN

Description

The SP1005 includes back-to-back Zener diodes fabricated in a proprietary silicon avalanche technology to provide protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes above the maximum level specified in the IEC61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. The back-to-back configuration provides symmetrical ESD protection for data lines when AC signals are present.

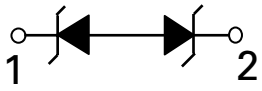
Pinout



Features

- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 10A (t_p=8/20μs)
- Low capacitance of 30pF (@ V_R=0V)
- Low leakage current of 0.1μA at 5V
- Industries smallest ESD footprint available (0201)

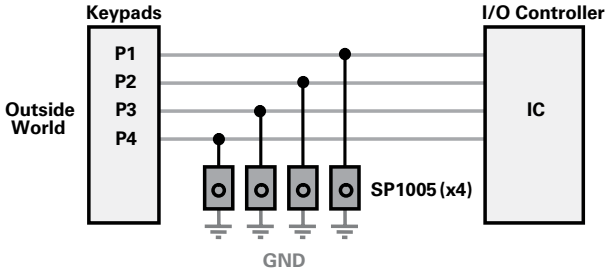
Functional Block Diagram



Applications

- Mobile phones
- Smart phones
- Camcorders
- PDA
- Digital cameras
- MP3/PMP
- Portable navigation devices
- Portable medical
- Point of sale terminals

Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	10.0	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-65 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}				6.0	V
Voltage Drop	V_D	I_R=1mA		8.5	9.5	V
Leakage Current	I_{LEAK}	V_R=5V with 1 pin at GND		0.1	0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		9.3		V
		I_{PP}=2A, t_p=8/20µs, Fwd		10.0		V
		I_{PP}=10A, t_p=8/20µs, Fwd		15.6		V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		0.7		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact Discharge)	±30			kV
		IEC61000-4-2 (Air Discharge)	±30			kV
Diode Capacitance[1]	C_D	Reverse Bias=0V		30		pF
		Reverse Bias=2.5V		23		pF

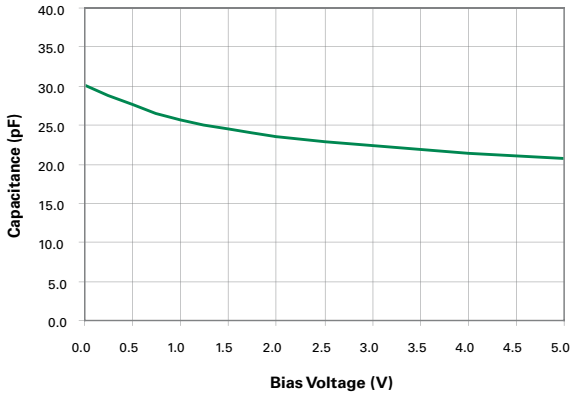
Note:
[1]Parameter is guaranteed by design and/or device characterization.

Product Characteristics

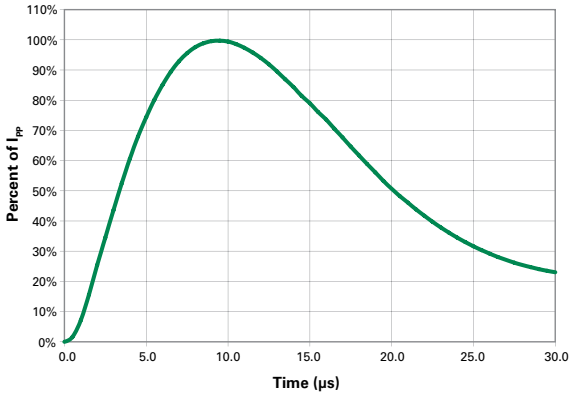
Lead Plating	Sn
Lead Material	Copper
Lead Coplanarity	6 um (max)
Subsitute Material	Silicon
Body Material	Silicon

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

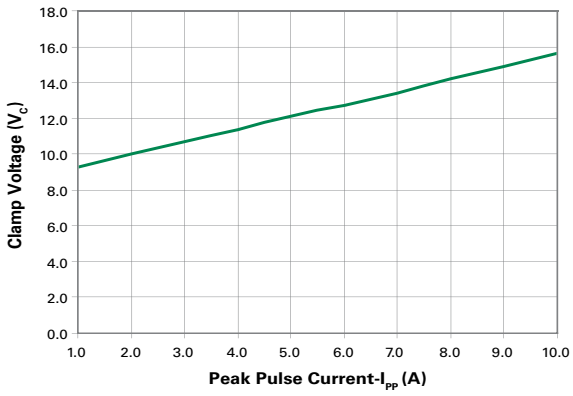
Capacitance vs. Reverse Bias



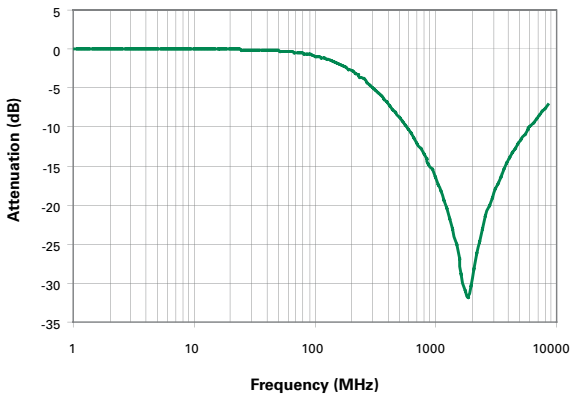
Pulse Waveform



Clamping Voltage vs. I_{PP}

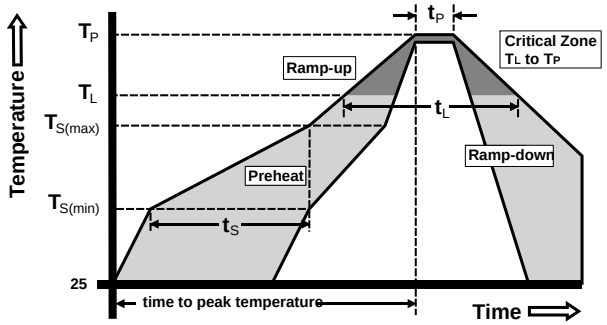


Insertion Loss (S21) I/O to GND

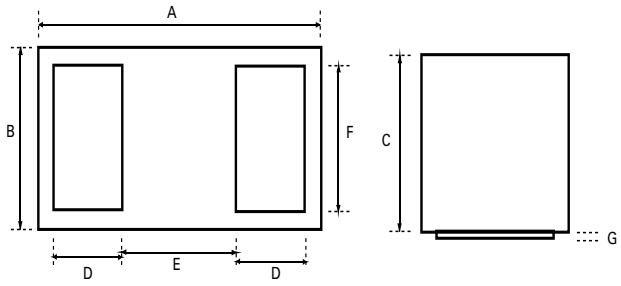


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

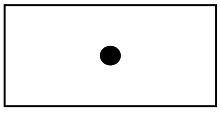


Package Dimensions — 0201 Flipchip



Symbol	0201 Flipchip					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.595	0.620	0.645	0.0234	0.0244	0.0254
B	0.295	0.320	0.345	0.0116	0.0126	0.0136
C	0.245	0.275	0.305	0.0096	0.0108	0.0120
D	0.145	0.150	0.155	0.0057	0.0059	0.0061
E	0.245	0.250	0.255	0.0096	0.0098	0.0100
F	0.245	0.250	0.255	0.0096	0.0098	0.0100
G	0.005	0.010	0.015	0.0002	0.0004	0.0006

Part Marking System



Part Numbering System

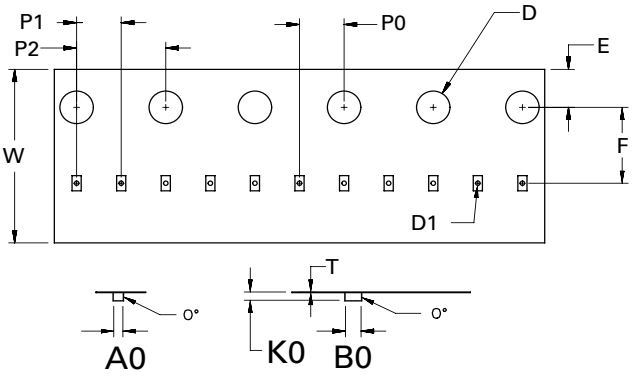
SP 1005 - 01 W T G

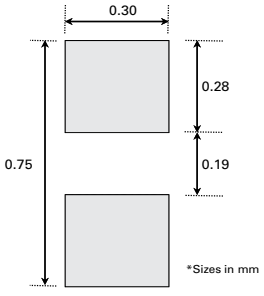
- SP: Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- 1005: Series
- 01: Number of Channels
- W: Package W: 0201 Flipchip
- T: T= Tape & Reel
- G: G= Green

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP1005-01WTG	0201 Flipchip	•	10000

Embossed Carrier Tape & Reel Specification — 0201 Flipchip





Recommended Solder Pad Footprint

Symbol	Millimeters
A0	0.41+/-0.03
B0	0.70+/-0.03
D	ø 1.50 + 0.10
D1	ø 0.20 +/- 0.05
E	1.75+/-0.10
F	3.50+/-0.05
K0	0.38+/-0.03
P0	2.00+/-0.05
P1	2.00+/-0.05
P2	4.00+/-0.10
W	8.00 + 0.30 -0.10
T	0.23+/-0.02

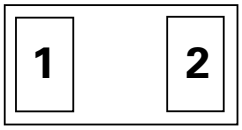
SP1007 Series 3.5pF 8kV Bidirectional Discrete TVS

HF RoHS GREEN

Description

The SP1007 includes back-to-back Zener diodes fabricated in a proprietary silicon avalanche technology to provide protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. The back-to-back configuration provides symmetrical ESD protection for data lines when AC signals are present.

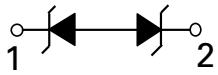
Pinout



Features

- ESD, IEC61000-4-2, ±8kV contact, ±15kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 2A (t_p=8/20µs)
- Low capacitance of 3.5pF (@ V_R=5V)
- Low leakage current of 0.1µA at 5V
- Industries smallest ESD footprint available (0201)

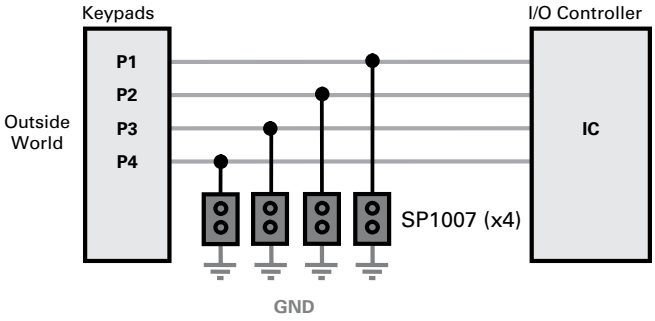
Functional Block Diagram



Applications

- Mobile phones
- Smart phones
- Camcorders
- PDA
- Digital cameras
- MP3/PMP
- Portable navigation devices
- Portable medical
- Point of sale terminals

Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	2.0	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-65 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

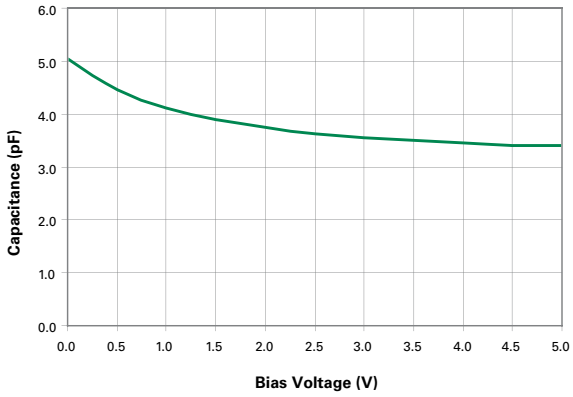
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

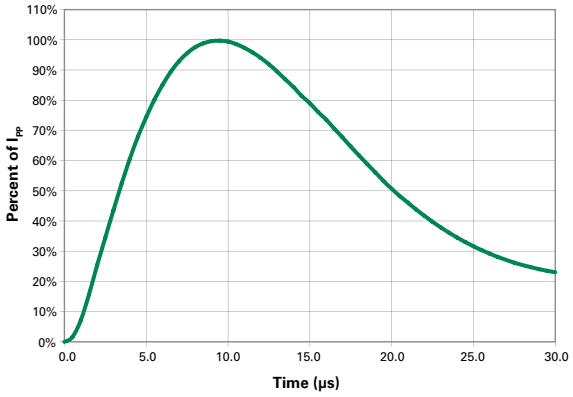
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}				6.0	V
Breakdown Voltage	V_{BR}	I_R=1mA		8.5	9.5	V
Leakage Current	I_{LEAK}	V_R=5V with 1 pin at GND		0.1	0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		10.3		V
		I_{PP}=2A, t_p=8/20µs, Fwd		12.2		V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		1.9		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact Discharge)	±8			kV
		IEC61000-4-2 (Air Discharge)	±15			kV
I/O to I/O Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		5	6	pF
		Reverse Bias=5.0V		3.5		pF

Note:
[1]Parameter is guaranteed by design and/or device characterization.

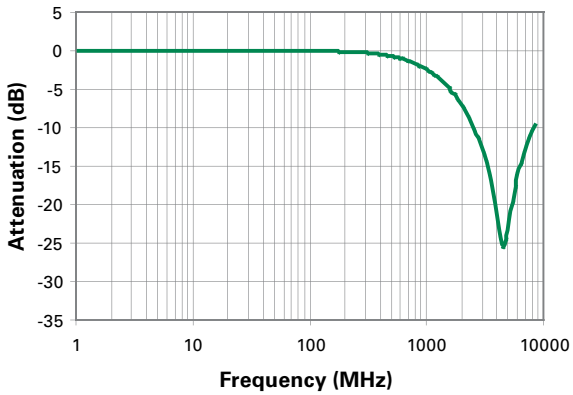
Capacitance vs. Reverse Bias



Pulse Waveform

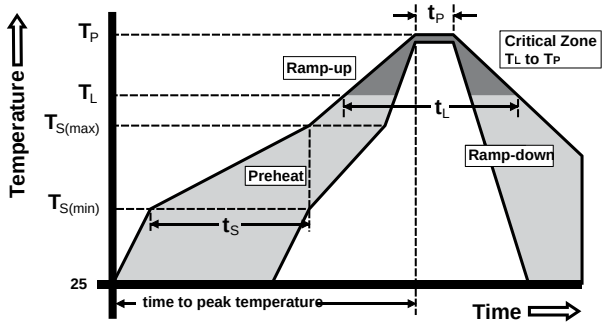


Insertion Loss (S21) I/O to GND

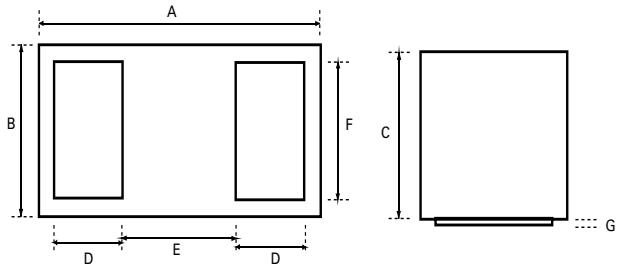


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — 0201 Flip Chip



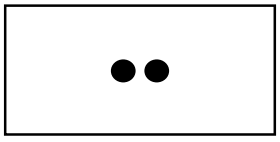
Symbol	0201 Flipchip					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.595	0.620	0.645	0.0234	0.0244	0.0254
B	0.295	0.320	0.345	0.0116	0.0126	0.0136
C	0.245	0.275	0.305	0.0096	0.0108	0.0120
D	0.145	0.150	0.155	0.0057	0.0059	0.0061
E	0.245	0.250	0.255	0.0096	0.0098	0.0100
F	0.245	0.250	0.255	0.0096	0.0098	0.0100
G	0.005	0.010	0.015	0.0002	0.0004	0.0006

Part Numbering System

SP 1007 - 01 W T G

- SP: Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- 1007: Series
- 01: Number of Channels
- W: Package W: 0201 Flipchip
- T: T= Tape & Reel
- G: G= Green

Part Marking System



Product Characteristics

Lead Plating	Sn
Lead Material	Copper
Lead Coplanarity	6 um (max)
Subsitute Material	Silicon
Body Material	Silicon

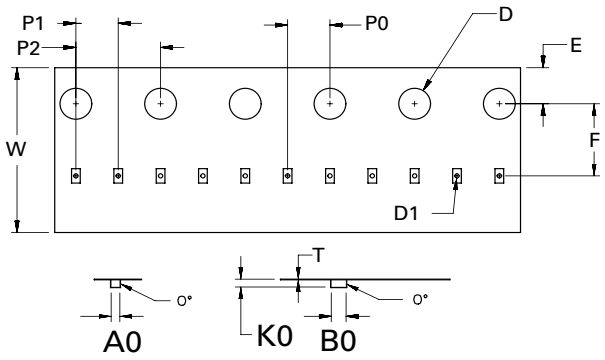
Notes :

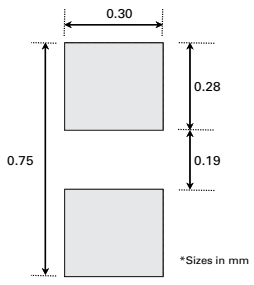
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP1007-01WTG	0201 Flipchip	• •	10000

Embossed Carrier Tape & Reel Specification — 0201 Flipchip



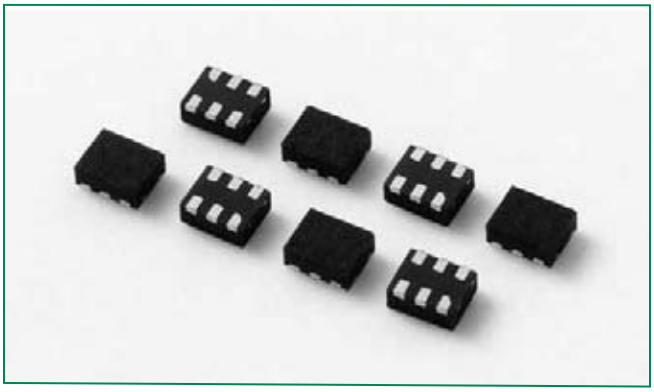


Recommended Solder Pad Footprint

Symbol	Millimeters
A0	0.41+/-0.03
B0	0.70+/-0.03
D	ø 1.50 + 0.10
D1	ø 0.20 +/- 0.05
E	1.75+/-0.10
F	3.50+/-0.05
K0	0.38+/-0.03
P0	2.00+/-0.05
P1	2.00+/-0.05
P2	4.00+/-0.10
W	8.00 + 0.30 -0.10
T	0.23+/-0.02

SP1010 Series 3.5pF 8kV Unidirectional TVS Array

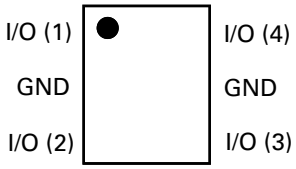
HF RoHS GREEN



Description

Zener diodes fabricated in a proprietary silicon avalanche technology protect each I/O pin to provide a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protection high-speed signal pins.

Pinout

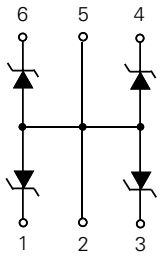


uDFN-6
(1.25x1.0x0.5mm)

Features

- ESD, IEC61000-4-2, ±8kV contact, ±15kV air
- Lightning, IEC61000-4-5, 1A (t_p=8/20μs)
- Low capacitance of 3.5pF (TYP) per I/O
- Low leakage current of 1μA (MAX) at 5V
- Tiny uDFN package (1.25mm x 1.0mm x 0.5mm)
- EFT protection IEC61000-4-4, 40A (5/50ns)

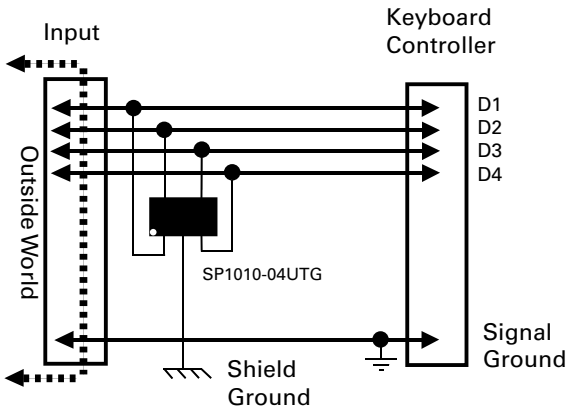
Functional Block Diagram



Applications

- Notebook
- Netbook
- Ultra mobile PC
- Mobile phone
- Portable navigation device
- Portable medical device
- MP3/PMP
- Digital camera

Application Example



Life Support Note:
Not Intended for Use in Life Support or Life Saving Applications
The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current (t_p=8/20μs)	1.0	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

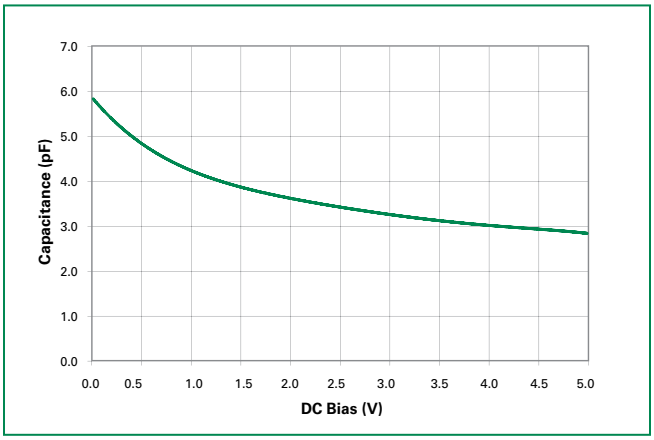
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

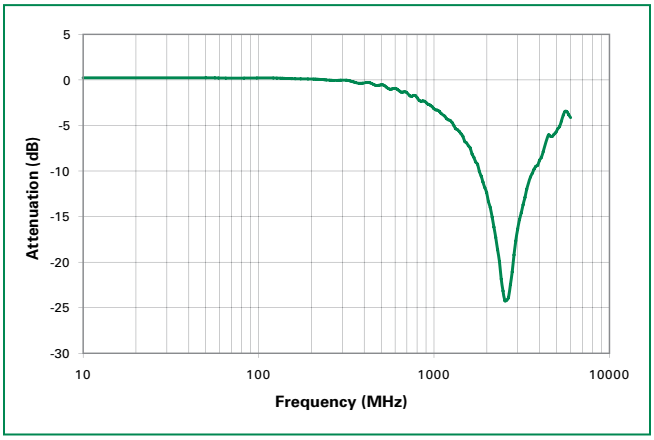
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Voltage Drop	V_R	I_R = 1mA	7.0	7.8	8.5	V
Reverse Standoff Voltage	V_{RWM}	I_R≤1μA			6	V
Reverse Leakage Current	I_{LEAK}	V_R = 5V		0.1	1	μA
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact Discharge)	±8			kV
		IEC61000-4-2 (Air Discharge)	±15			kV
Diode Capacitance[1]	C_D	Reverse Bias = 0V		6	7	pF
		Reverse Bias = 2.5V		3.5		pF

Note:
1. Parameter is guaranteed by design and/or device characterization.

Capacitance vs. Reverse Bias

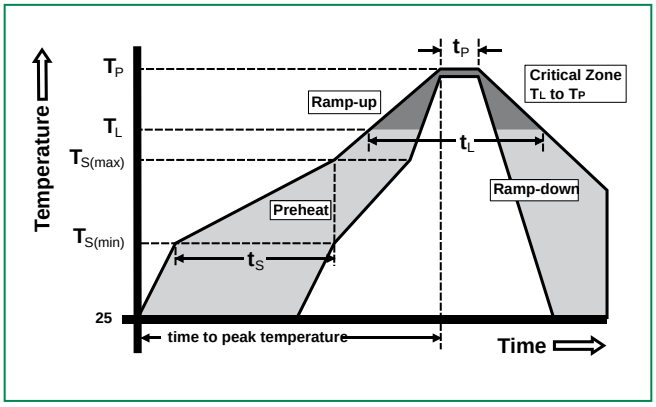


Insertion Loss (S21) I/O to GND

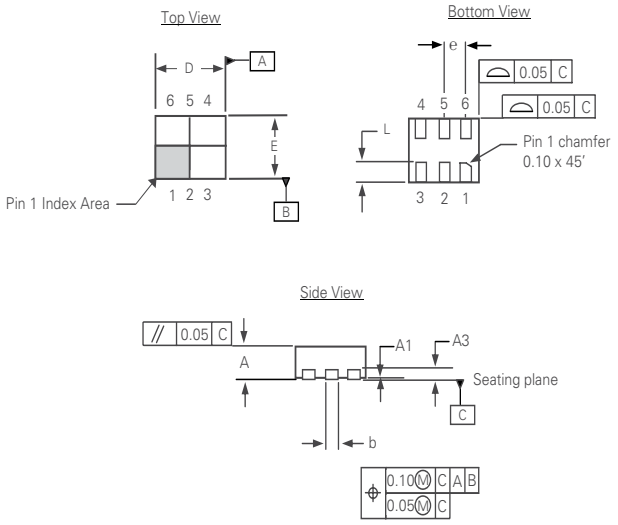


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		260$^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

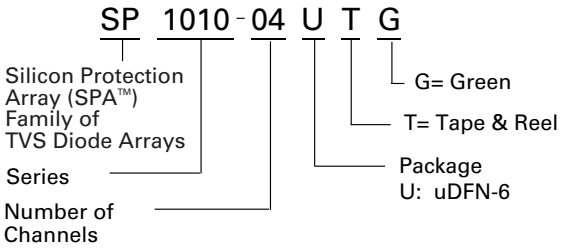


Package Dimensions — uDFN-6 (1.25x1.0x0.5mm)

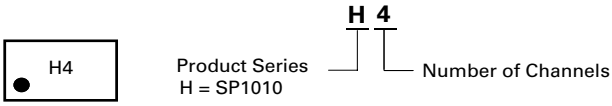


uDFN-6 (1.25x1.0x0.5mm)				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
A3	0.127 REF		0.005 REF	
b	0.15	0.25	0.006	0.010
D	1.20	1.30	0.047	0.051
D2	-	-	-	-
E	0.95	1.05	0.037	0.041
E2	-	-	-	-
e	0.4 REF		0.016 REF	
L	0.25	0.35	0.010	0.014

Part Numbering System



Part Marking System



Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

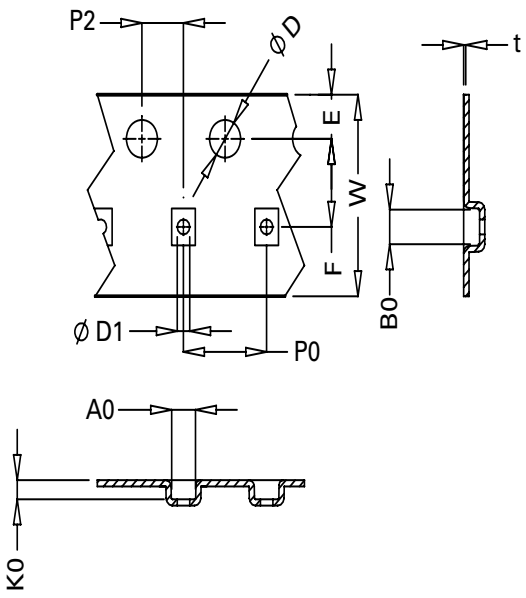
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP1010-04UTG	uDFN-6 (1.25x1.0x0.5mm)	H4	3000

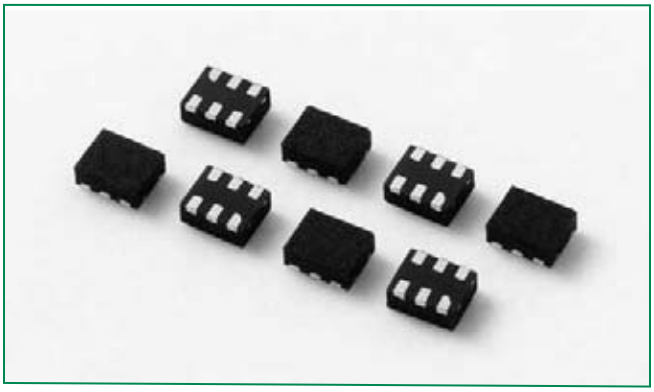
Embossed Carrier Tape & Reel Specification — uDFN-6 (1.25x1.0x0.5mm)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.06	0.07
F	3.45	3.55	0.14	0.14
D1	0.50	0.65	0.02	0.03
D	1.50 MIN		0.06 MIN	
P0	3.90	4.10	0.15	0.16
10P0	40.0 +/- 0.20		1.57 +/- 0.01	
W	7.90	8.30	0.31	0.33
P2	1.95	2.05	0.08	0.08
A0	1.09	1.19	0.04	0.05
B0	1.42	1.52	0.06	0.06
K0	0.71	0.81	0.03	0.03
t	0.25 TYP		0.01 TYP	

SP1011 Series 7pF 15kV Unidirectional TVS Array

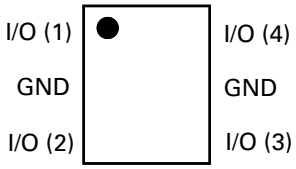
HF RoHS GREEN



Description

Zener diodes fabricated in a proprietary silicon avalanche technology protect each I/O pin to provide a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protection high-speed signal pins.

Pinout

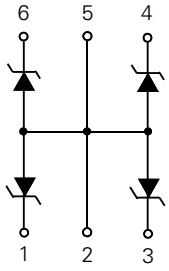


uDFN-6
(1.25x1.0x0.5mm)

Features

- ESD, IEC61000-4-2, ±15kV contact, ±30kV air
- Lightning, IEC61000-4-5, 2A (t_p=8/20μs)
- Low capacitance of 7 pF (TYP) per I/O @ 2.5V
- Low leakage current of 1μA (MAX) at 5V
- Tiny uDFN package (1.25mm x 1.0mm x 0.5mm)
- EFT protection IEC61000-4-4, 40A (5/50ns)

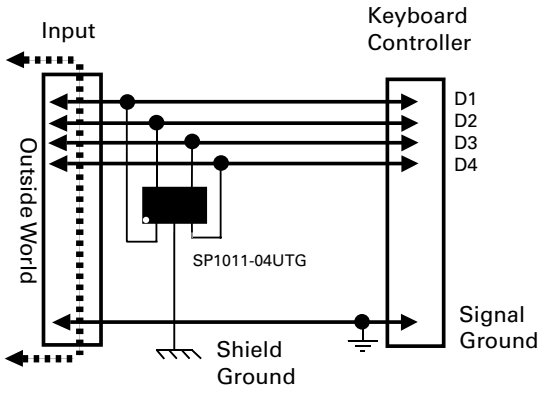
Functional Block Diagram



Applications

- LCD/PDP TV
- DVD Player
- Desktop
- Set Top Box
- Mobile Phone
- Notebook
- MP3/PMP
- Digital camera

Application Example



Life Support Note:
Not Intended for Use in Life Support or Life Saving Applications
The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current (t_p=8/20µs)	2	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

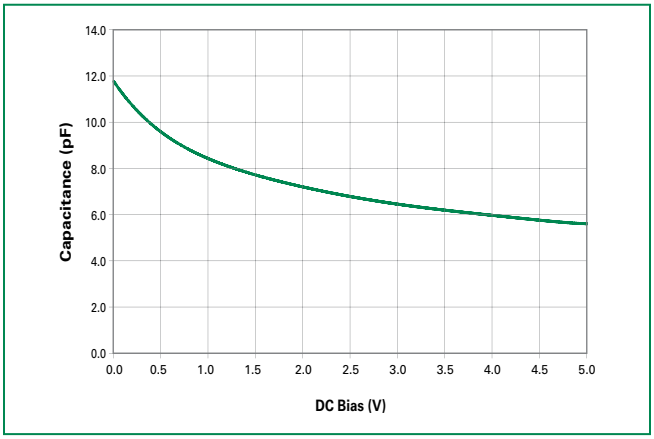
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

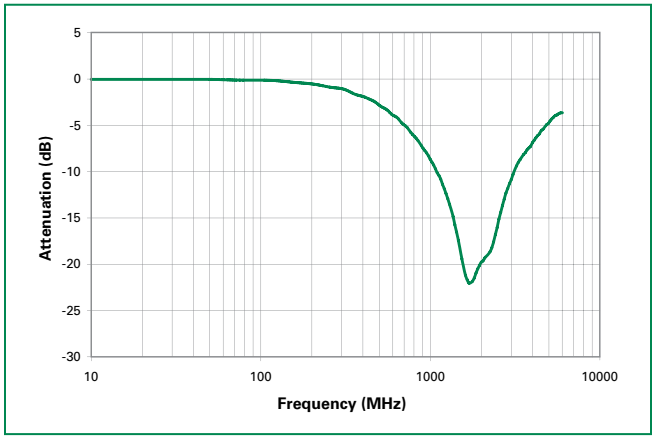
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Voltage Drop	V_R	I_R = 1mA	7.0	7.8	8.5	V
Reverse Standoff Voltage	V_{RWM}	I_R≤1µA			6	V
Reverse Leakage Current	I_{LEAK}	V_R = 5V		0.1	1	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		8.7		V
		I_{PP}=2A, t_p=8/20µs, Fwd		10.2		V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		1.5		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact Discharge)	±15			kV
		IEC61000-4-2 (Air Discharge)	±30			kV
Diode Capacitance[1]	C_D	Reverse Bias = 0V		12	15	pF
		Reverse Bias = 2.5V		7		pF

Note:
1. Parameter is guaranteed by design and/or device characterization.

Capacitance vs. Reverse Bias

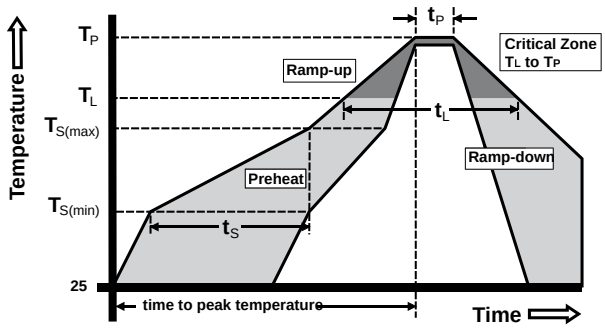


Insertion Loss (S21) I/O to GND

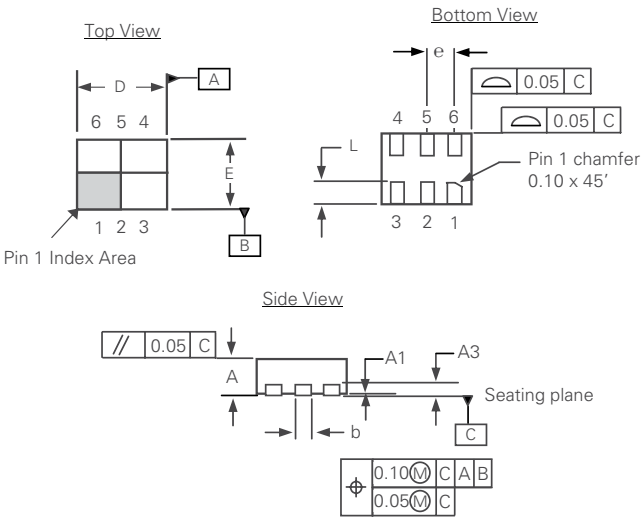


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

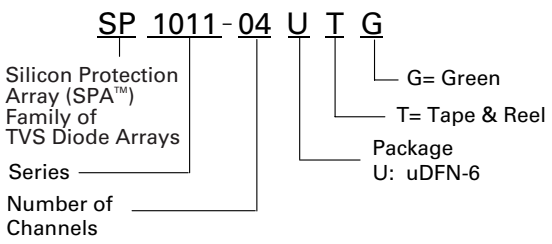


Package Dimensions — uDFN-6 (1.25x1.0x0.5mm)



uDFN-6 (1.25x1.0x0.5mm)				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
A3	0.127 REF		0.005 REF	
b	0.15	0.25	0.006	0.010
D	1.20	1.30	0.047	0.051
D2	-	-	-	-
E	0.95	1.05	0.037	0.041
E2	-	-	-	-
e	0.4 REF		0.016 REF	
L	0.25	0.35	0.010	0.014

Part Numbering System



Part Marking System

Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

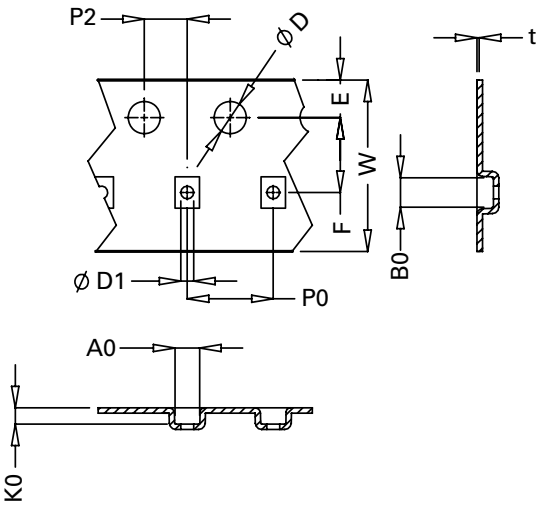
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP1011-04UTG	uDFN-6 (1.25x1.0x0.5mm)	O4	3000

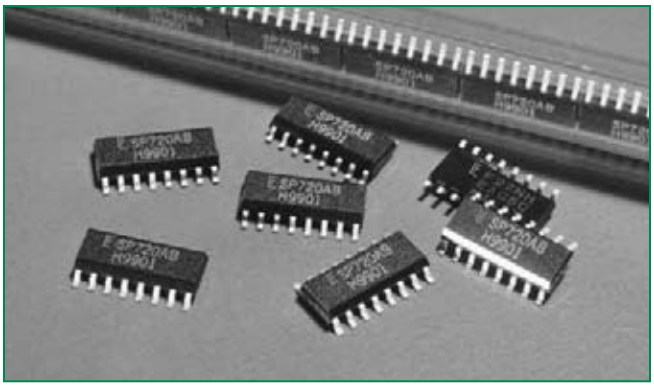
Embossed Carrier Tape & Reel Specification — uDFN-6 (1.25x1.0x0.5mm)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.06	0.07
F	3.45	3.55	0.14	0.14
D1	0.50	0.65	0.02	0.03
D	1.50 MIN		0.06 MIN	
P0	3.90	4.10	0.15	0.16
10P0	40.0 +/- 0.20		1.57 +/- 0.01	
W	7.90	8.30	0.31	0.33
P2	1.95	2.05	0.08	0.08
A0	1.09	1.19	0.04	0.05
B0	1.42	1.52	0.06	0.06
K0	0.71	0.81	0.03	0.03
t	0.25 TYP		0.01 TYP	

SP720 Series 3pF 4kV Rail Clamp Array

RoHS GREEN



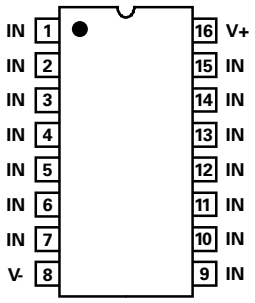
Description

The SP720 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP720 has 2 protection SCR/Diode device structures per input. A total of 14 available inputs can be used to protect up to 14 external signal or bus lines. Over-voltage protection is from the IN (pins 1-7 and 9-15) to V+ or V-.

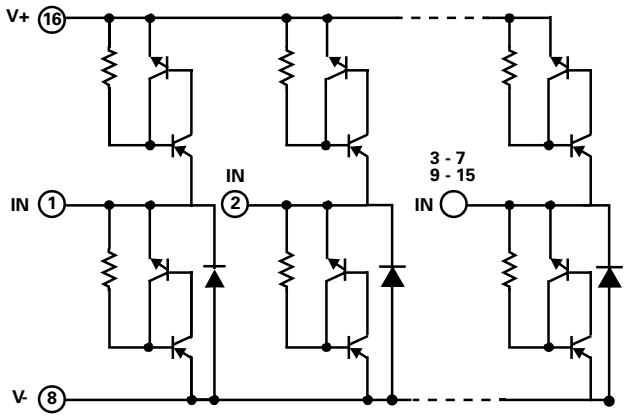
The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 16) or a $-V_{BE}$ diode threshold below V- (Pin 8). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

Pinout

SP720 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Features

- ESD Interface Capability for HBM Standards
  - MIL STD 3015.7 ..... 15kV
  - IEC 61000-4-2, Direct Discharge,
  - Single Input ..... 4kV (Level 2)
  - Two Inputs in Parallel ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge ..... 15kV (Level 4)
- High Peak Current Capability
  - IEC 61000-4-5 (8/20µs) ..... ±3A
  - Single Pulse, 100µs Pulse Width ..... ±2A
  - Single Pulse, 4µs Pulse Width ..... ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching ..... 2ns Risetime
- Low Input Leakages ..... 1nA at 25° (Typ)
- Low Input Capacitance ..... 3pF (Typ)
- An Array of 14 SCR/Diode Pairs
- Operating Temperature Range ..... -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Life Support Note:
Not Intended for Use in Life Support or Life Saving Applications
The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND (Refer to Figure 5)	±2, 100µs	A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:

ESD Ratings and Capability - See Figure 1, Table 1
Load Dump and Reverse Battery (Note 2)

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
PDIP Package	90	°C/W
SOIC Package	130	°C/W
Maximum Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature (Plastic Package)	150	°C
Maximum Lead Temperature (Soldering 20-40s) (SOIC Lead Tips Only)	260	°C

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC}, Unless Otherwise Specified

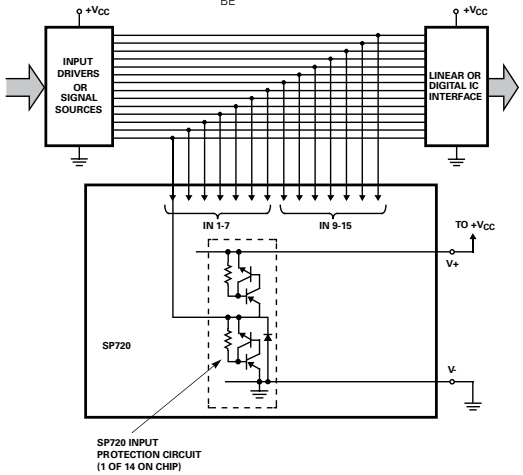
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop:		I_{IN} = 1A (Peak Pulse)				
IN to V-	V_{FWDL}		-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

Notes:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and everse battery V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP720 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance." These characteristics are given here for thumb-rule nformation to determine peak current and dissipation under EOS conditions.

Typical Application of the SP720

(Application as an Input Clamp for Over-voltage, greater than 1V_{BE} Above V+ or less than -1V_{BE} below V-)



ESD Capability

ESD capability is dependent on the application and defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP720 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 6kV. The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 61000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2). Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP720 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

Figure 1: Electrostatic Discharge Test

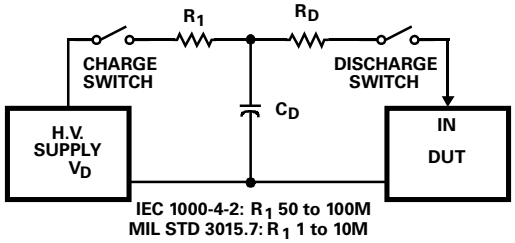


Table 1: ESD Test Conditions

Standard	Type/Mode	R_D	C_D	$\pm V_D$
MIL STD 3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 61000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

Figure 2: Low Current SCR Forward Voltage Drop Curve

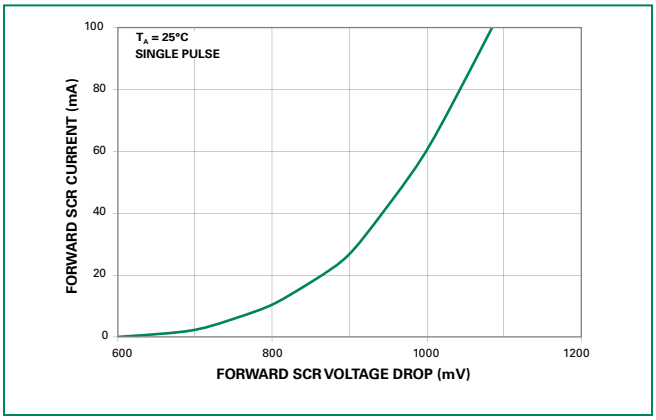
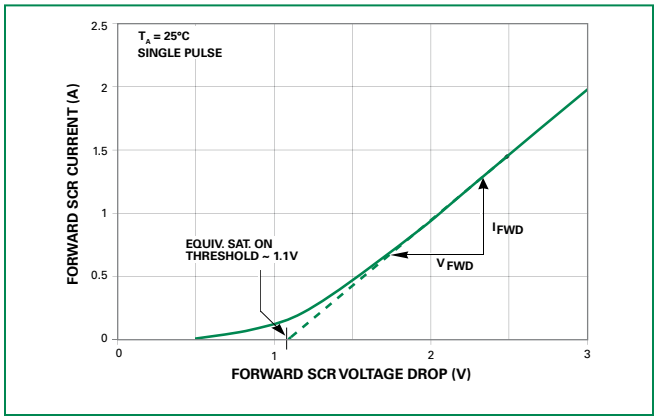


Figure 3: High Current SCR Forward Voltage Drop Curve



Peak Transient Current Capability for Long Duration Surges

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP720's ability to withstand a wide range of transient current pulses. The circuit used to generate current pulses is shown in Figure 4.

The test circuit of Figure 4 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP720 'IN' input pin and the (+) current pulse input goes to the SP720 V- pin. The V+ to V- supply of the SP720 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 5 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the V+ to V- voltage supply level, improving as the supply voltage is reduced. Values of 0, 5, 15 and 30 voltages are shown. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in Figure 5.

When adjacent input pins are paralleled, the sustained peak current capability is increased to nearly twice that of a single pin. For comparison, tests were run using dual pin combinations 1+2, 3+4, 5+6, 7+9, 10+11, 12+13 and 14+15.

The overstress curve is shown in Figure 5 for a 15V supply condition. The dual pins are capable of 10A peak current for a 10µs pulse and 4A peak current for a 1ms pulse. The complete for single pulse peak current vs. pulse width time ranging up to 1 second are shown in Figure 5.

Figure 4: Typical SP720 Peak Current Test Circuit with a Variable Pulse Width Input

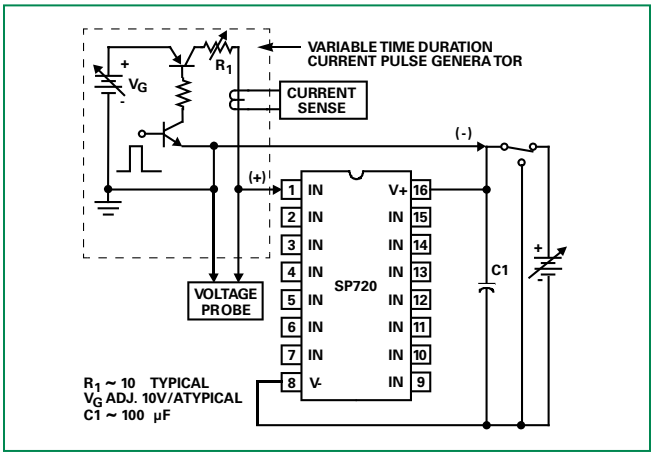
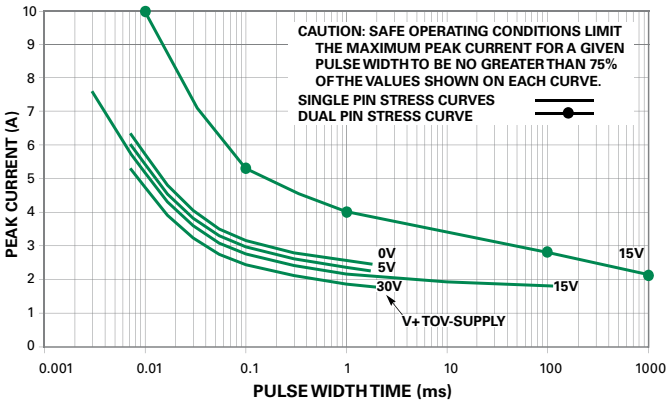


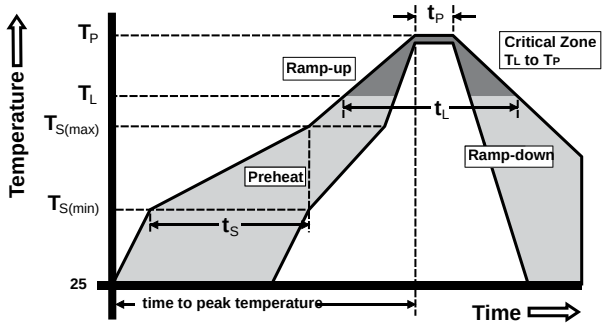
Figure 5: SP720 Typical Nonrepetitive Peak Current Pulse Capability

Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds (T_A = 25°C)



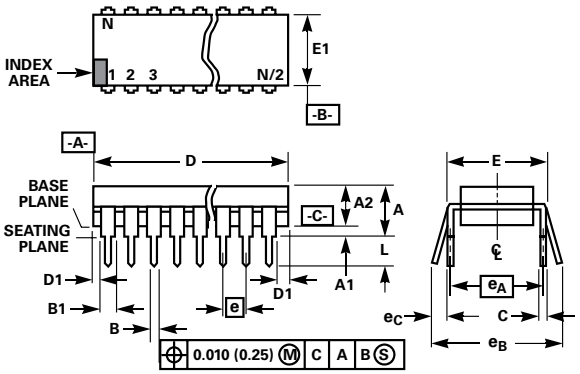
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Lead-Free/Green SP720

Package Dimensions Dual-In-Line Plastic Packages (PDIP)

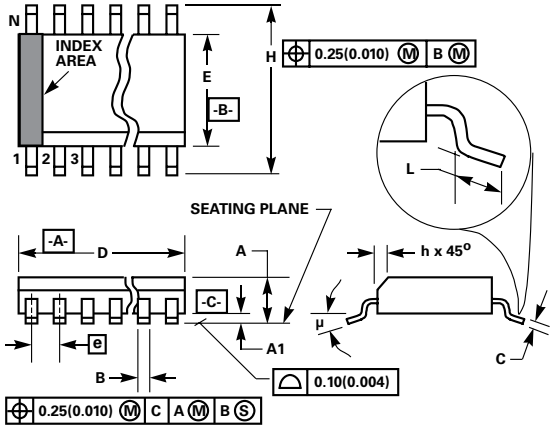


Notes:

1. Controlling Dimensions: INCH. in case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JE-DEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_c are measured at the lead tips with the leads unconstrained. e_c must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Package	PDIP				
Pins	16 Lead Dual-in-Line				
JEDEC	E16.3 MS-001-BB Issue D				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	-	5.33	-	0.210	4
A1	0.39	-	0.015	-	4
A2	2.93	4.95	0.115	0.195	-
B	0.356	0.558	0.014	0.022	-
B1	1.15	1.77	0.045	0.070	8, 10
C	0.204	0.355	0.008	0.014	-
D	18.66	19.68	0.735	0.775	5
D1	0.13	-	0.005	-	5
E	7.62	8.25	0.300	0.325	6
E1	6.10	7.11	0.240	0.280	5
e	2.54 BSC		0.100 BSC		-
e_A	7.62 BSC		0.300 BSC		6
e_B	-	10.92	-	0.430	7
L	2.93	3.81	0.115	0.150	4
N	16		16		9

Package Dimensions — Small Outline Plastic Packages (SOIC)



Package	SOIC				
Pins	16				
JEDEC	M16.15 (JEDEC MS-012-AC Issue C)				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	1.35	1.75	0.0532	0.0688	-
A1	0.10	0.25	0.0040	0.0098	-
B	0.33	0.51	0.013	0.020	9
C	0.19	0.25	0.0075	0.0098	-
D	9.80	10.00	0.3859	0.3937	3
E	3.80	4.00	0.1497	0.1574	4
e	1.27 BSC		0.050 BSC		-
H	5.80	6.20	0.2284	0.2440	-
h	0.25	0.50	0.0099	0.0196	5
L	0.40	1.27	0.016	0.050	6
N	16		16		7
μ	0°	8°	0°	8°	-

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension:MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System

SP720ABTG

- SP720 — Silicon Protection Array (SPA™) Family of TVS Diode Arrays — Series
- AB — Package: AB = 16 Ld SOIC; AP = 16 Ld PDIP
- TG — P=Lead Free; G = Green; TG= Tape and Reel / Green

See Ordering Information section for specific options available

Product Characteristics

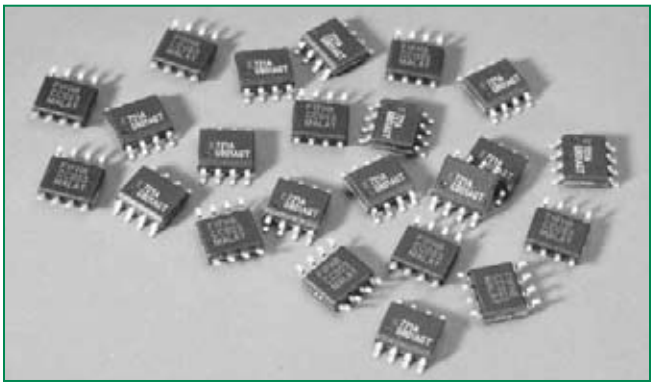
Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Ordering Information

Part Number	Temp. Range (°C)	Package	Environmental Informaton	Marking	Min. Order
SP720APP	-40 to 105	16 Ld PDIP	Lead-free	720APP	1500
SP720ABG	-40 to 105	16 Ld SOIC	Green	720ABG	1920
SP720ABTG	-40 to 105	16 Ld SOIC Tape and Reel	Green	720ABG	2500

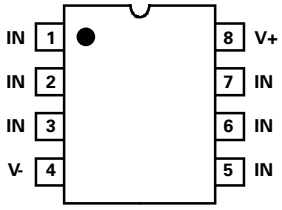
SP721 Series 3pF 4kV Rail Clamp Array

RoHS GREEN

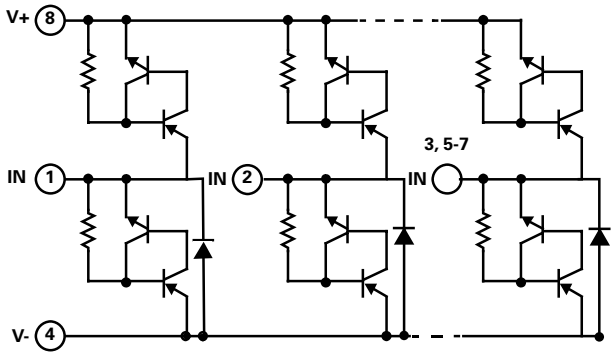


Pinout

SP721 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Description

The SP721 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP721 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

Features

- ESD Interface Capability for HBM Standards
  - MIL STD 3015.7 ..... 15kV
  - IEC 61000-4-2, Direct Discharge,
  - Single Input ..... 4kV (Level 2)
  - Two Inputs in Parallel ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge ..... 15kV (Level 4)
- High Peak Current Capability
  - IEC 61000-4-5 (8/20µs) ..... ±3A
  - Single Pulse, 100µs Pulse Width ..... ±2A
  - Single Pulse, 4µs Pulse Width ..... ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching ..... 2ns Rise Time
- Low Input Leakages ..... 1nA at 25°C Typical
- Low Input Capacitance ..... 3pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range ..... -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND (Refer to Figure 5)	±2, 100µs	A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:

ESD Ratings and Capability (Figure 1, Table 1)

Load Dump and Reverse Battery (Note 2)

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
PDIP Package	160	°C/W
SOIC Package	170	°C/W
Maximum Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature (Plastic Package)	150	°C
Maximum Lead Temperature (Soldering 20-40s)(SOIC Lead Tips Only)	260	°C

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

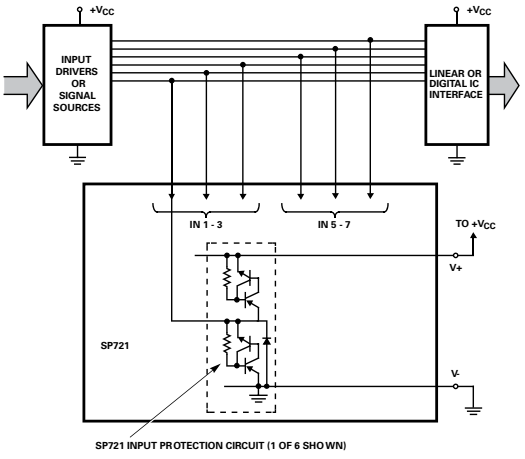
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range,	V_{SUPPLY}		-	2 to 30	-	V
V_{SUPPLY} = [(V+) - (V-)]						
Forward Voltage Drop						
IN to V-	V_{FWDL}	I_{IN} = 1A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	1	-	W
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

Notes:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to het same supply voltage source as the device or control line under protection, a current limiti ng resistor should be connected in series between the external supply and the SP721 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger romf the V+ and V- Pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule nformation to determine peak current and dissipation under EOS conditions.

Typical Application of the SP721

(Application as an Input Clamp for Over-voltage, Greater than 1V_{BE} Above V+ or less than -1V_{BE} below V-)



ESD Capability

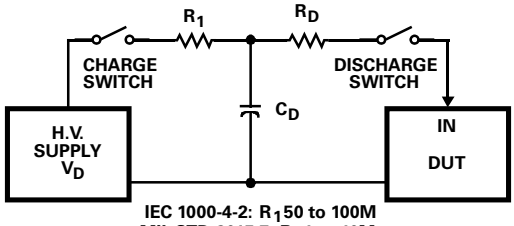
ESD capability is dependent on the application and defined test standard.The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified"MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP721 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ.By strict definition of MIL-STD-3015.7 using "pin-to-pin"device testing, the ESD voltage capability is greater than 6kV.The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 61000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2).Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP721 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

Figure 1: Electrostatic Discharge Test



IEC 1000-4-2: R1 50 to 100M
MIL-STD-3015.7: R1 1 to 10M

Table 1: ESD Test Conditions

Standard	Type/Mode	R_D	C_D	$\pm V_D$
MIL STD 3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 61000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

Figure 2: Low Current SCR Forward Voltage Drop Curve

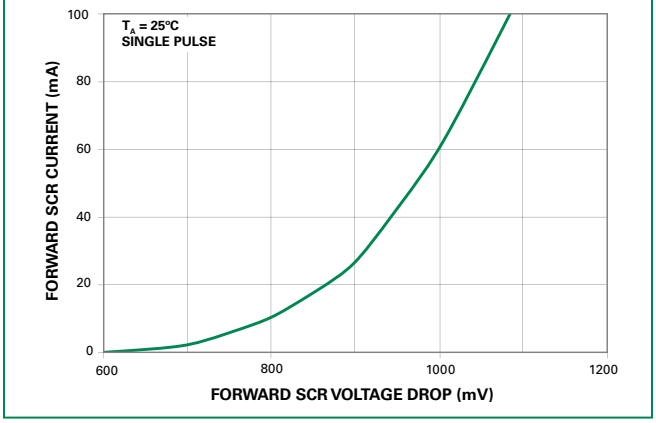
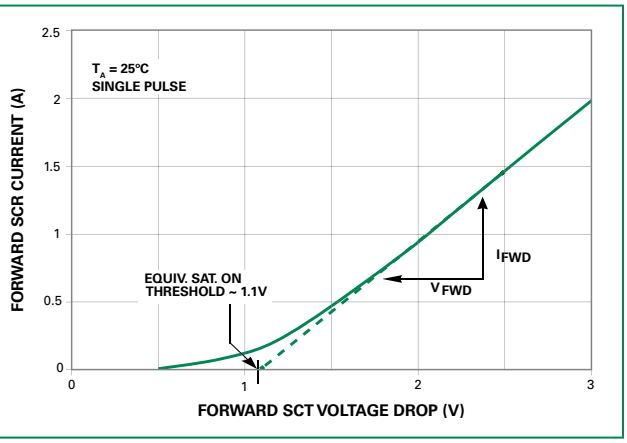


Figure 3: High Current SCR Forward Voltage Drop Curve



Peak Transient Current Capability of the SP721

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP721's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 4.

The test circuit of Figure 4 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP721 'IN' input pin and the (+) current pulse input goes to the SP721 V- pin. The V+ to V- supply of the SP721 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 5 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25ºC and 105ºC and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 5.

Note that adjacent input pins of the SP721 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

Figure 4: Typical SP721 Peak Current Test Circuit with a Variable Pulse Width Input

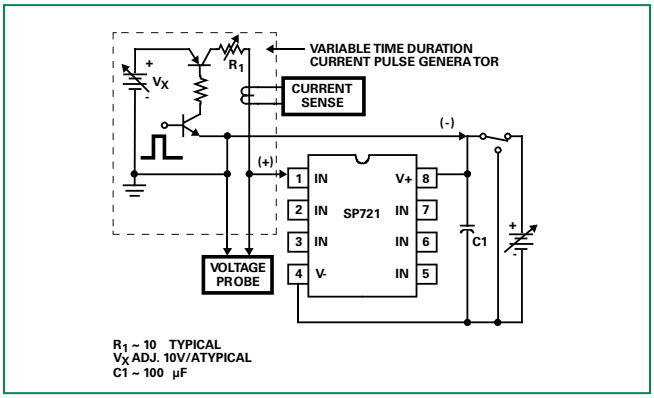
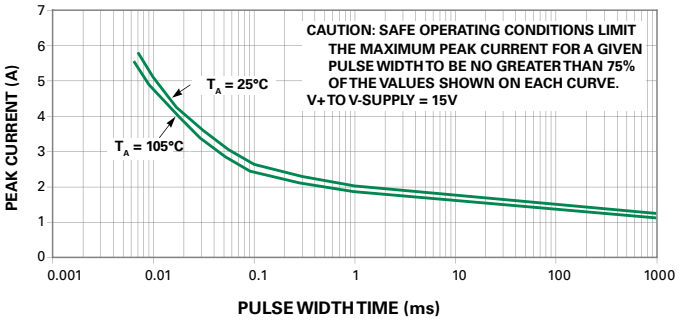


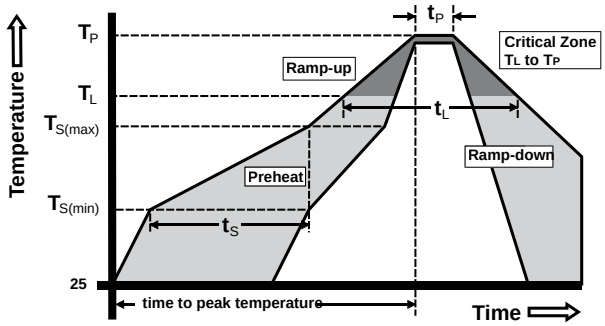
Figure 5: SP721 Typical Single Peak Current Pulse Capability

Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds

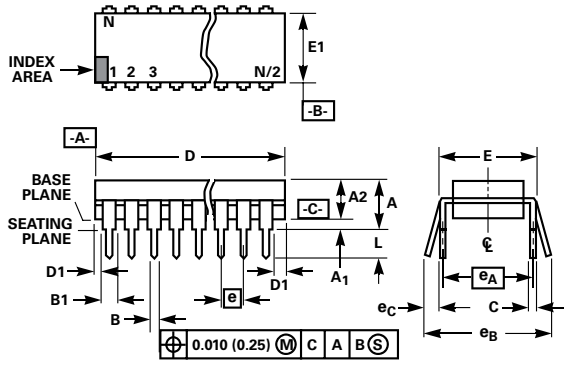


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — Dual-In-Line Plastic Packages (PDIP)

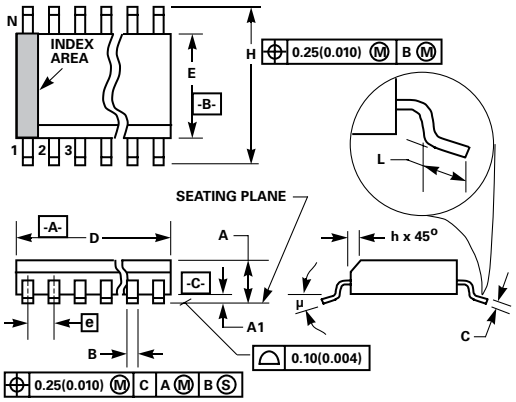


Notes:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is t he maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Package	PDIP				
Pins	8 Lead Dual-in-Line				
JEDEC	E8.3 MS-001-BA Issue D				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	-	5.33	-	0.210	4
A1	0.39	-	0.015	-	4
A2	2.93	4.95	0.115	0.195	-
B	0.356	0.558	0.014	0.022	-
B1	1.15	1.77	0.045	0.070	8, 10
C	0.204	0.355	0.008	0.014	-
D	9.01	10.16	0.355	0.400	5
D1	0.13	-	0.005	-	5
E	7.62	8.25	0.300	0.325	6
E1	6.10	7.11	0.240	0.280	5
e	2.54 BSC		0.100 BSC		-
e_A	7.62 BSC		0.300 BSC		6
e_B	-	10.92	-	0.430	7
L	2.93	3.81	0.115	0.150	4
N	8		8		9

Package Dimensions — Small Outline Plastic Packages (SOIC)

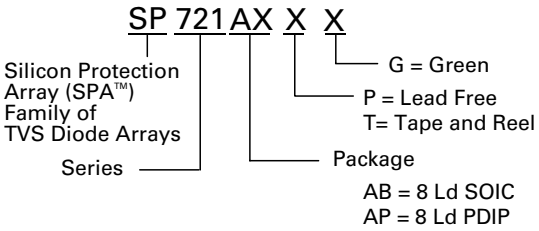


Package	SOIC				
Pins	8				
JEDEC	M8.15 (JEDEC MS-012-AA Issue C)				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	1.35	1.75	0.0532	0.0688	-
A1	0.10	0.25	0.0040	0.0098	-
B	0.33	0.51	0.013	0.020	9
C	0.19	0.25	0.0075	0.0098	-
D	4.80	5.00	0.1890	0.1968	3
E	3.80	4.00	0.1497	0.1574	4
e	1.27 BSC		0.050 BSC		-
H	5.80	6.20	0.2284	0.2440	-
h	0.25	0.50	0.0099	0.0196	5
L	0.40	1.27	0.016	0.050	6
N	8		8		7
μ	0°	8°	0°	8°	-

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System



Product Characteristics

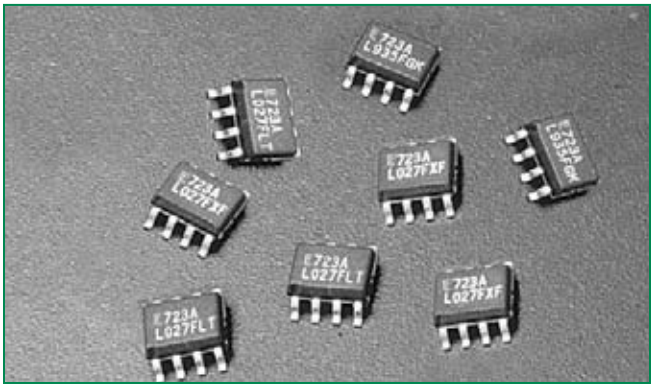
Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Ordering Information

Part Number	Temp. Range (°C)	Package	Environmental Informaton	Marking	Min. Order
SP721APP	-40 to 105	8 Ld PDIP	Lead-free	721APP	2000
SP721ABG	-40 to 105	8 Ld SOIC	Green	721AG	1960
SP721ABTG	-40 to 105	8 Ld SOIC Tape and Reel	Green	721AG	2500

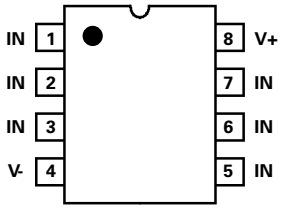
SP723 Series 5pF 8kV Rail Clamp Array

RoHS GREEN

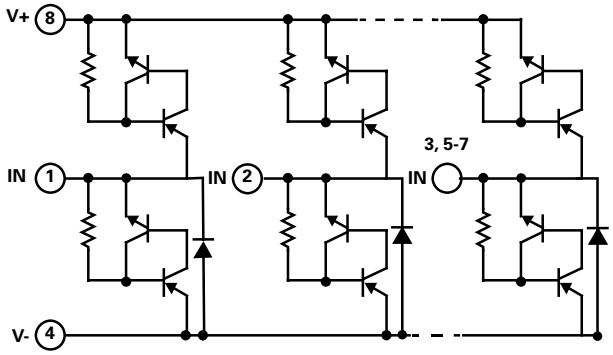


Pinout

SP723 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Description

The SP723 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection of sensitive input circuits. The SP723 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

Refer to Fig 1 and Table 1 for further details. Refer to Application Note AN9304 and AN9612 for further detail.

Features

- ESD Interface per HBM Standards
  - IEC 61000-4-2, Direct Discharge ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge.....15kV (Level 4)
  - MIL-STD-3015.7 .....25kV
- Peak Current Capability
  - IEC 61000-4-5 8/20µs Peak Pulse Current..... ±7A
  - Single Transient Pulse, 100s Pulse Width ..... ±4A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching.....2ns Risetime
- Low Input Leakages.....2nA at 25°C Typical
- Low Input Capacitance.....5pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range.....-40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Life Support Note:
Not Intended for Use in Life Support or Life Saving Applications
The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND (Refer to Figure 5)	±4, 100µs	A
Peak Pulse Current, 8/20µs	±7	A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:

ESD Ratings and Capability (Figure 1, Table 1)

Load Dump and Reverse Battery (Note 2)

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
PDIP Package	160	°C/W
SOIC Package	170	°C/W
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature (Plastic Package)	150	°C
Lead Temperature (Soldering 20-40s) (SOIC Lead Tips Only)	260	°C

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

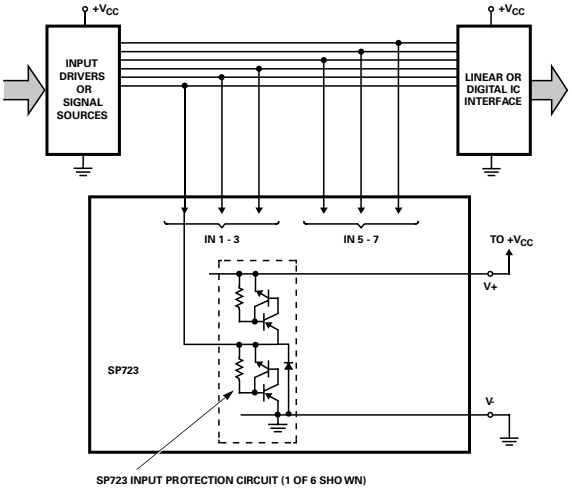
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{SUPPLY} =[(V+)-(V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop						
IN to V-	V_{FWDL}	I_{IN}=2A(Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshod		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	0.5	-	Ω
Input Capacitance	C_{IN}		-	5	-	PF
Input Switching Speed	t_{ON}		-	2	-	ns

Notes:

2. In automotive ans battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, acurrent limiting resistor should be connected in series between the external supply and the SP723 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- Pins to ground are recommended.
3. Refer to the Figure 3 graph for determine peak current and dessipation under EOS conditions.

Typical Application of the SP723

(Application as an Input Clamp for Over-voltage, Greater than 1V_{BE} Above V+ or less than -1V_{BE} below V-)



SP723 INPUT PROTECTION CIRCUIT (1 OF 6 SHOWN)

ESD Capability

ESD capability is dependent on the application and defined test standard.The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

The SP723 has a Level 4 HBM capability when tested as a device to the IEC 61000-4-2 standard. Level 4 specifies a required capability greater than 8kV for direct discharge and greater than 15kV for air discharge.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP723 ESD capability is typically greater than 25kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 10kV.

For the SP723 EIAJ IC121 Machine Model (MM) standard, the ESD capability is typically greater than 2kV from 200pF with no series resistance.

Figure 1: Electrostatic Discharge Test

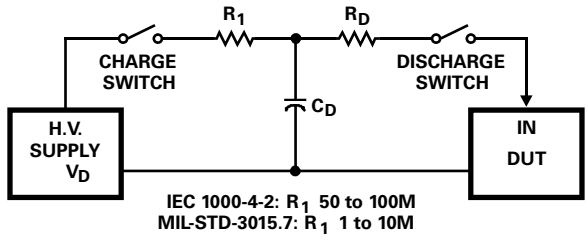


Table 1: ESD Test Conditions

Standard	Type/Mode	R_D	C_D	$\pm V_D$
IEC 1000-4-2 (Level 4)	HBM, Air Discharge	330 Ω	150pF	15kV
	HBM, Direct Discharge	330 Ω	150pF	8kV
MIL-STD-3015.7	Modified HBM	1.5k Ω	100pF	25kV
	Standard HBM	1.5k Ω	100pF	10kV
EIAJ IC121	Machine Model	0k Ω	200pF	2kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

Figure 2: Low Current SCR Forward Voltage Drop Curve

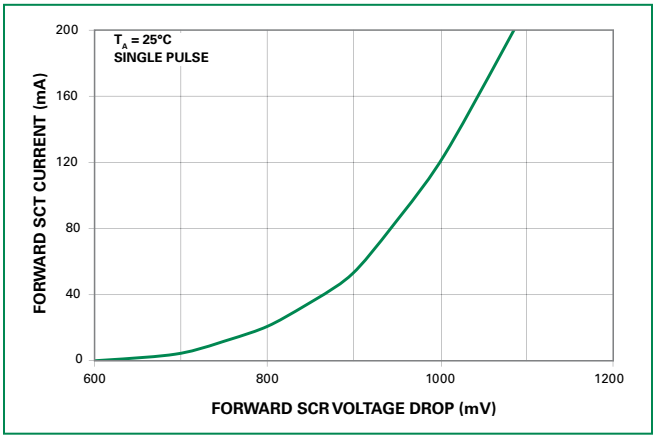
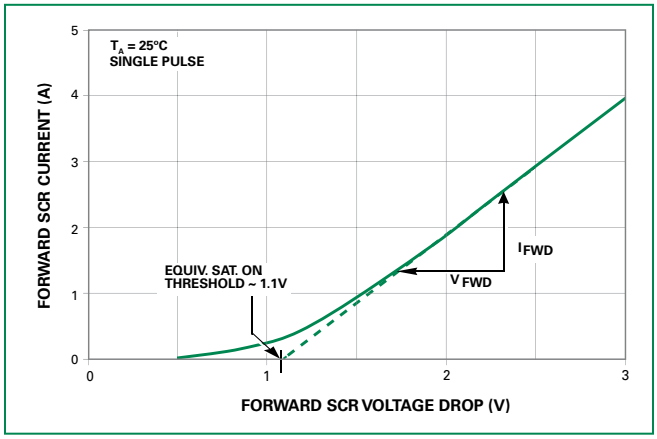


Figure 3: High Current SCR Forward Voltage Drop Curve



Peak Transient Current Capability of the SP723

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP723's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 4.

The test circuit of Figure 4 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP723 'IN' input pin and the (+) current pulse input goes to the SP723 V- pin. The V+ to V- supply of the SP723 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 5 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25ºC and 105ºC and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 5.

Note that adjacent input pins of the SP723 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

Figure 4: Typical SP723 Peak Current Test Circuit with a Variable Pulse Width Input

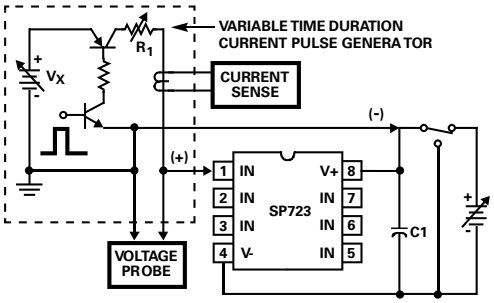
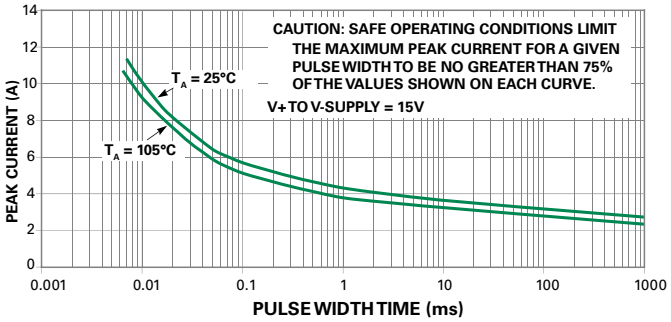


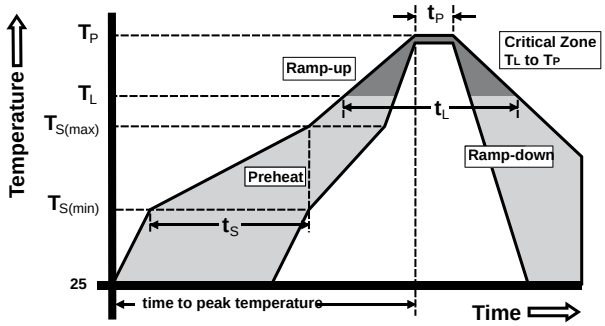
Figure 5: SP723 Typical Single Peak Current Pulse Capability

Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds



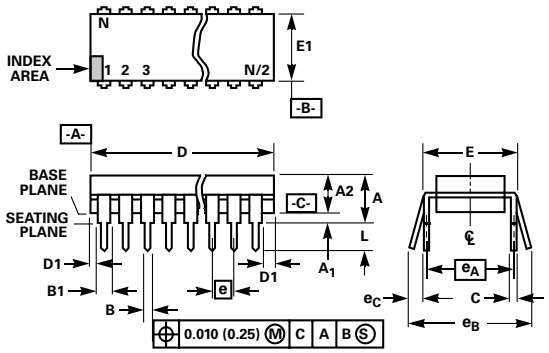
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Lead-Free/Green SP723

Package Dimensions — Dual-In-Line Plastic Packages (PDIP)

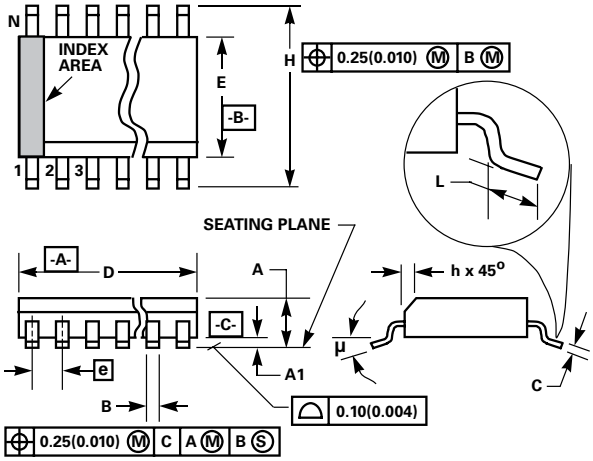


Package	PDIP				
Pins	8				
JEDEC	E8.3 (JEDEC MS-001-BA Issue D)				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	-	5.33	-	0.210	4
A1	0.39	-	0.015	-	4
A2	2.93	4.95	0.115	0.195	-
B	0.356	0.558	0.014	0.022	-
B1	1.15	1.77	0.045	0.070	8, 10
C	0.204	0.355	0.008	0.014	-
D	9.01	10.16	0.355	0.400	5
D1	0.13	-	0.005	-	5
E	7.62	8.25	0.300	0.325	6
E1	6.1	7.11	0.240	0.280	5
e	2.54 BSC		0.100 BSC		-
e_A	7.62 BSC		0.300 BSC		6
e_B	-	10.92	-	0.430	7
L	2.93	3.81	0.115	0.150	4
N	8		8		9

Notes:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads unconstrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads uncon-strained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Package Dimensions — Small Outline Plastic Packages (SOIC)



Package	SOIC				
Pins	8				
JEDEC	M8.15 (JEDEC MS-012-AA Issue C)				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	1.35	1.75	0.0532	0.0688	-
A1	0.10	0.25	0.0040	0.0098	-
B	0.33	0.51	0.013	0.020	9
C	0.19	0.25	0.0075	0.0098	-
D	4.80	5.00	0.1890	0.1968	3
E	3.80	4.00	0.1497	0.1574	4
e	1.27 BSC		0.050 BSC		-
H	5.80	6.20	0.2284	0.2440	-
h	0.25	0.50	0.0099	0.0196	5
L	0.40	1.27	0.016	0.050	6
N	8		8		7
μ	0°	8°	0°	8°	-

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The eadl width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension:MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System

SP 723 AX X X

- SP 723: Silicon Protection Array (SPA™) Family of TVS Diode Arrays Series
- AX: Package
  - AB = 8 Ld SOIC
  - AP = 8 Ld PDIP
- X: P=Lead Free, T= Tape and Reel
- X: G=Green

Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

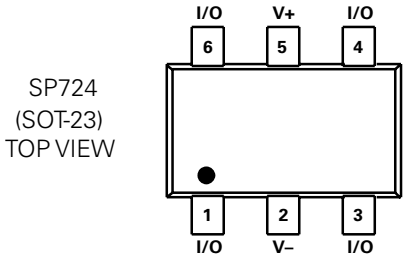
Ordering Information

Part Number	Temp. Range (°C)	Package	Environmental Informaton	Marking	Min. Order
SP723APP	-40 to 105	8 Ld PDIP	Lead-free	723APP	2000
SP723ABG	-40 to 105	8 Ld SOIC	Green	723AG	1960
SP723ABTG	-40 to 105	8 Ld SOIC Tape and Reel	Green	723AG	2500

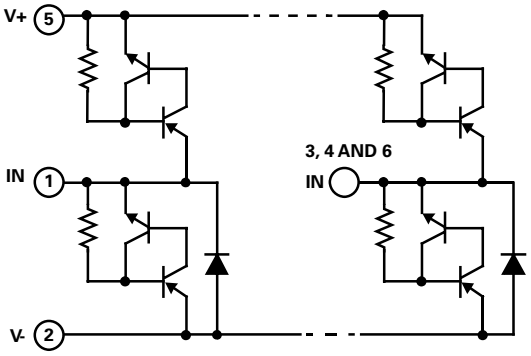
SP724 Series 3pF 8kV Rail Clamp Array

RoHS GREEN

Pinout



Functional Block Diagram



Notes:

1. The design of the SP724 SCR/Diode ESD Protection Arrays are covered by Littelfuse patent 4567500.
2. The full ESD capability of the SP724 is achieved when wired in a circuit that includes connection to both the V+ and V- pins. When handling individual devices, follow proper procedures for electrostatic discharge.

Description

The SP724 is a quad array of transient voltage clamping circuits designed to suppress ESD and other transient over-voltage events. The SP724 is used to help protect sensitive digital or analog input circuits on data, signal, or control lines operating on power supplies up to 20VDC.

The SP724 is comprised of bipolar SCR/diode structures to protect up to four independent lines by clamping transients of either polarity to the power supply rails. The SP724 offers very low leakage (1nA Typical) and low input capacitance (3pF Typical). Additionally, the SP724 is rated to withstand the IEC 61000-4-2 ESD specification for both contact and air discharge methods to level 4.

The SP724 is connected to the sensitive input line and its associated power supply lines. Clamping action occurs during the transient pulse, turning on the diode and fast triggering SCR structures when the voltage on the input line exceeds one V_{BE} threshold above the V+ supply (or one V_{BE} threshold below the V- supply). Therefore, the SP724P operation is unaffected by poor power supply regulation or voltage fluctuations within its operating range.

Features

- An Array of 4 SCR/Diode Pairs in 6-Lead SOT-23
- ESD Capability per HBM Standards
  - IEC 61000-4-2, Direct Discharge ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge.....15kV (Level 4)
  - MIL STD 3015.7..... >8kV
- Input Protection for Applications with Power Supplies Up to +20V (Single-Ended Voltage), and ±10V (Differential Voltage)
- Peak Current Capability
  - IEC 61000-4-5 (8/20µs) ..... ±3A
  - Single Pulse, 100µs Pulse Width ..... ±2.2A
- Low Input Leakage..... 1nA Typical
- Low Input Capacitance.....3pF Typical
- Operating Temperature Range.....-40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+20	V
Forward Peak Current, I_{IN} to V_{CC} , GND (Refer to Figure 5)	±2.2, 100µs	A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:

ESD Ratings and Capability - See Figure 1, Table 1

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 3)	θ_{JA}	°C/W
SOT Package	220	°C/W
Maximum Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s) (SOT - Lead Tips Only)	260	°C

Note: 3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

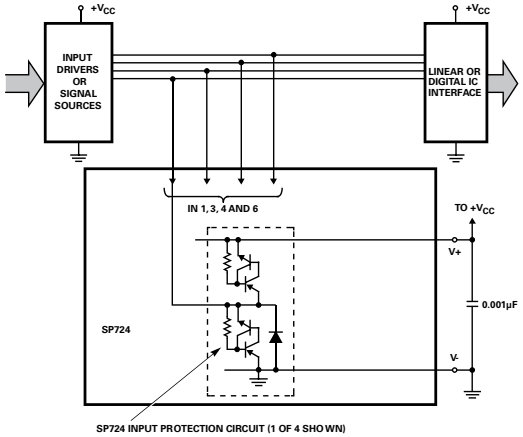
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)] (Notes 4, 5)	V_{SUPPLY}		1	-	20	V
Forward Voltage Drop						
Forward Voltage Drop IN to V-	V_{FWDL}	I_{IN} = 1A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-10	1	10	nA
Quiescent Supply Current	$I_{QUIESCENT}$	V+ = 20V, V- = GND	-	-	100	nA
Equivalent SCR ON Threshold		(Note 6)	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} (Note 6)	-	1.0	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF

Notes:

4. In automotive and other battery charging systems, the SP724 power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP724 supply pins to limit reverse battery current to within the rated maximum limits.
5. Bypass capacitors of typically 0.01µF or larger should be connected closely between the V+ and V- Pins for all applications.
6. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for information to determine peak current and dissipation under EOS conditions.

Typical Application of the SP724

Application as an Input Clamp for Over-voltage, Greater than 1V_{BE} Above V+ or less than -1V_{BE} below V-)



ESD Capability

ESD rating is dependent on the defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.3

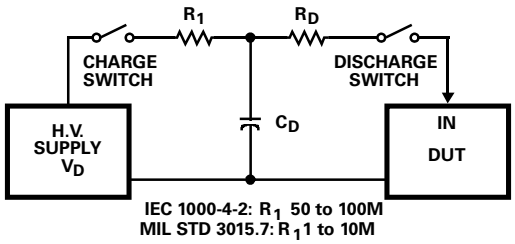
The SP724 has a Level 4 rating when tested to the IEC 61000-4-2 Human Body Model (HBM) standard and connected in a circuit in which the V+ and V- pins have a return path to ground. Level 4 specifies a required capability greater than 8kV for direct discharge and greater than 15kV for air discharge.

The "Modified" MIL-STD-3015.7 condition is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground.The SP724 ESD capability is greater than 8kV with 100pF discharged through 1.5kΩ. By strict definition of the standard MIL-STD-3015.7 method using "pin-to-pin" device testing, the ESD voltage capability is greater than 2kV.

For the SP724 EIAJ IC121 Machine Model (MM) standard, the ESD capability is typically greater than 1.8kV with 200pF discharged through 0kΩ.

The Charged Device model is based upon the self-capacitance of the SOT-23 package through 0kΩ.

Figure 1: Electrostatic Discharge Test



IEC 1000-4-2: R_1 50 to 100M
MIL STD 3015.7: R_1 1 to 10M

Table 1: ESD Test Conditions

Standard	Type/Mode	R_D	C_D	$\pm V_D$
IEC 61000-4-2 (Level 4)	HBM, Air Discharge	330 Ω	150pF	15kV
	HBM, Direct Discharge	330 Ω	150pF	8kV
MIL-STD-3015.7	Modified HBM	1.5k Ω	100pF	8kV †
	Standard HBM	1.5k Ω	100pF	2kV
EIAJ IC121	Machine Model	0k Ω	200pF	400V
US ESD DS 5.3	Charged Device Model	0k Ω	NA	3kV

†Upper limit of laboratory test set.

Figure 2: Low Current SCR Forward Voltage Drop Curve

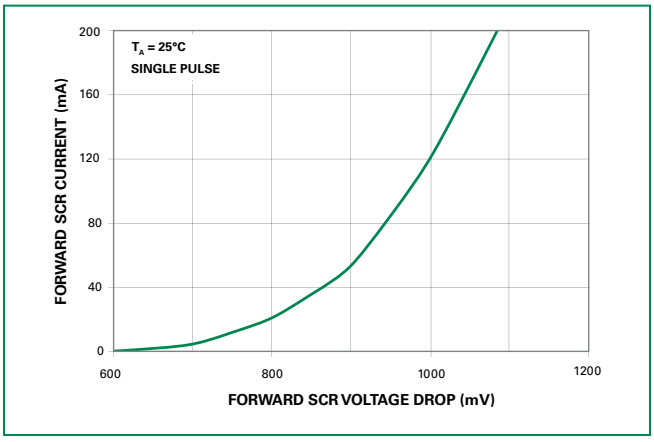
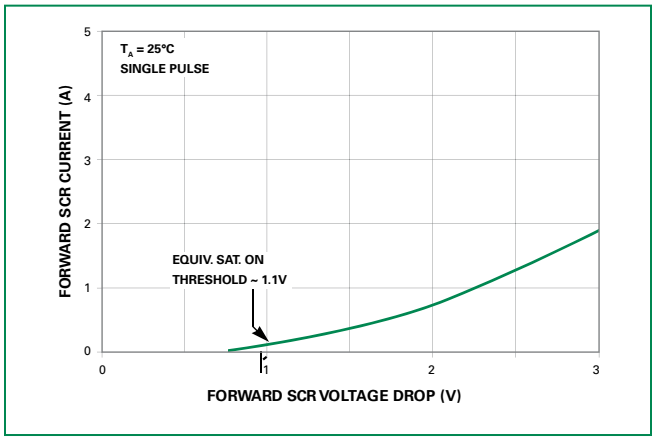


Figure 3: High Current SCR Forward Voltage Drop Curve



Peak Transient Current Capability for Long Duration Surges

The peak transient current capability is inversely proportional to the width of the current pulse. Testing was done to fully evaluate the SP724's ability to withstand long duration current pulses using the circuit of Figure 4. Figure 5 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curve of Figure 5.

The test circuit of Figure 4 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP724 'IN' input pin and the (+) current pulse input goes to the SP724 V- pin. The V+ to V- supply of the SP724 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.)

Note that two input pins of the SP724 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

Figure 4: Typical SP724 Peak Current Test Circuit with a Variable Pulse Width Input

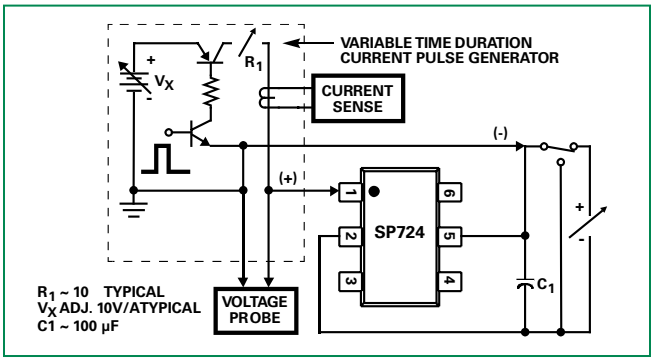
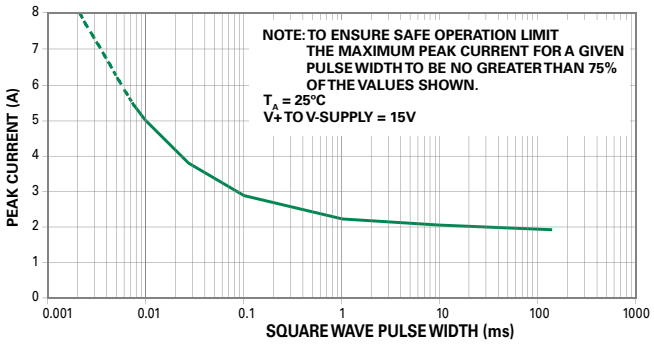


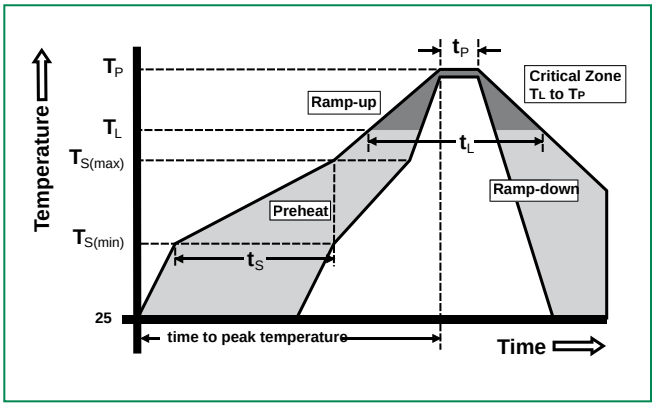
Figure 5: SP724 Typical Nonrepetitive Peak Current Pulse Capability

Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds

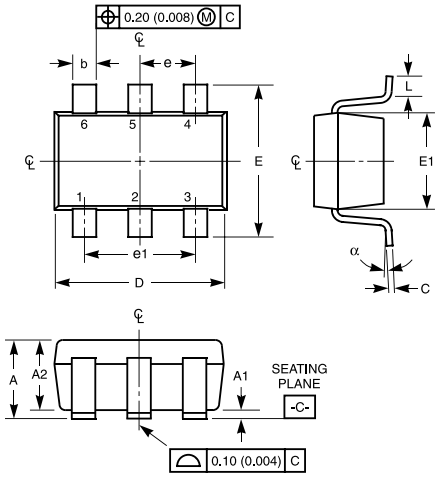


Soldering Parameters

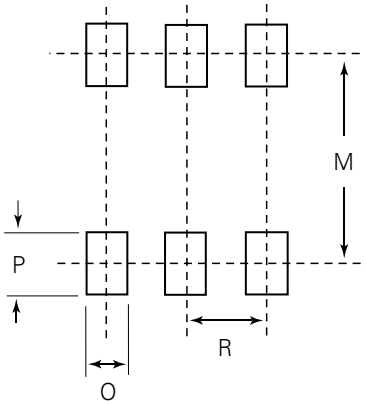
Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — Small Outline Transistor Plastic Packages (SOT23-6)



Recommended Solder Pad Layout



Package	SOT23-6				
Pins	6				
JEDEC	MO-203 Issue A				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	0.900	1.450	0.035	0.057	-
A1	0.000	0.150	0.000	0.006	-
A2	0.900	1.300	0.035	0.051	-
b	0.350	0.500	0.0138	0.0196	-
C	0.080	0.220	0.0031	0.009	-
D	2.800	3.000	0.11	0.118	3
E	2.600	3.000	0.102	0.118	-
E1	1.500	1.750	0.06	0.069	3
e	0.95 Ref		0.0374 ref		-
e1	1.9 Ref		0.0748 Ref		-
L	0.100	0.600	0.004	0.023	4,5
N	6		6		6
a	0°	10°	0°	10°	-
M		2.590		0.102	-
O		0.690		.027 TYP	-
P		0.990		.039 TYP	-
R		0.950		0.038	-

Notes:

1. Dimensioning and tolerances per ANSI 14.5M-1982.
2. Package conforms to EIAJ SC-74 (1992).
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlenth L measured at reference to seating plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System

SP 724 AH T G

- SP: Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- 724: Series
- AH: Package Type, AH: SOT-23
- T: Tape and Reel
- G: "Green" RoHS Compliant

Ordering Information

Part Number	Temp. Range (°C)	Package	Marking	Min. Order Qty.
SP724AHTG	-40 to 105	Tape and Reel	724G	3000

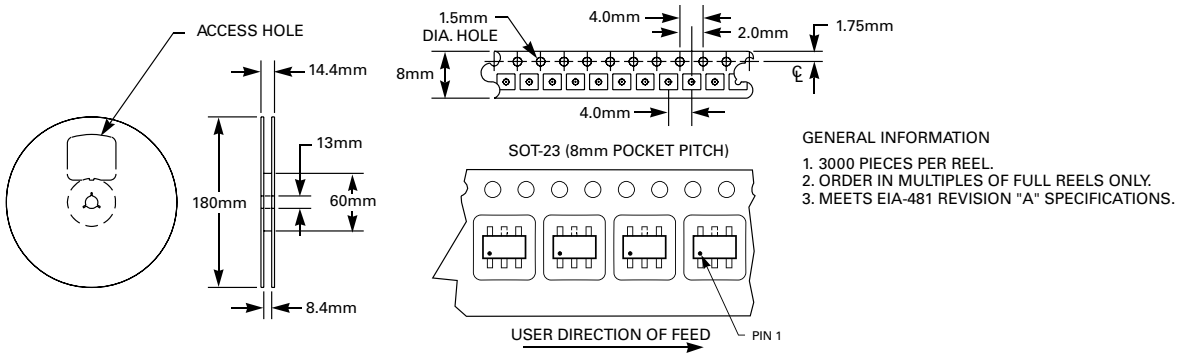
Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes:
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 ISSUE A.
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Embossed Carrier Tape & Reel Specification — SOT23-6

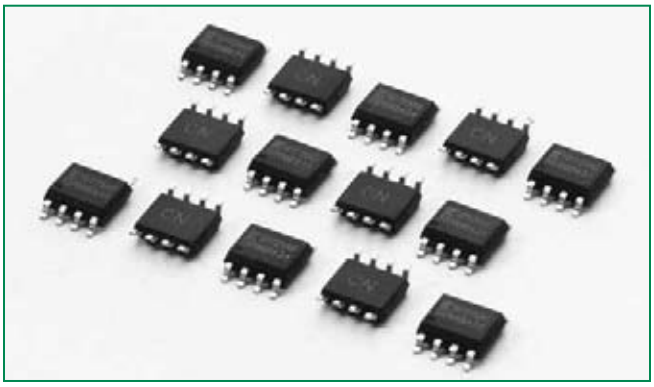
8mm TAPE AND REEL



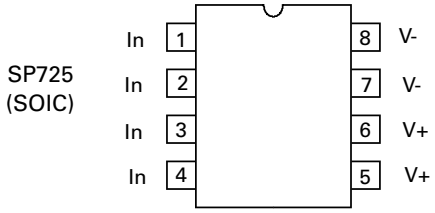
GENERAL INFORMATION
1. 3000 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

SP725 Series 5pF 8kV Rail Clamp Array

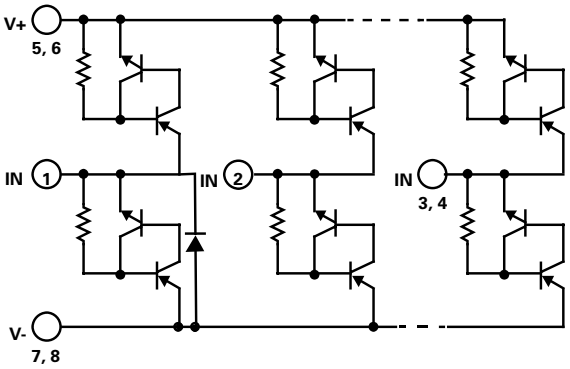
RoHS GREEN



Pinout



Functional Block Diagram



Description

The SP725 is an array of SCR/Diode bipolar structures for ESD and overvoltage protection of sensitive input circuits. The SP725 has 2 protection SCR/Diode device structures per input. There are a total of 4 available inputs that can be used to protect up to 4 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 4) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 5,6) or one $-V_{BE}$ diode threshold below V- (Pin 7,8). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

Refer to Fig 1 and Table 1 for further details. Refer to Application Note AN9304 and AN9612 for further detail.

Features

- ESD Interface per HBM Standards
  - IEC 61000-4-2, Direct Discharge ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge.....15kV (Level 4)
  - MIL-STD-3015.7 .....25kV
- Peak Current Capability
  - IEC 61000-4-5 8/20 µs Peak Pulse Current..... ± 14 A
  - Single Transient Pulse, 100 µs Pulse Width ..... ± 8 A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching.....2ns Risetime
- Low Input Leakages.....5 nA at 25 °C Typical
- Low Input Capacitance.....5 pF Typical
- An Array of 4 SCR/Diode Pairs
- Operating Temperature Range.....-40 °C to 105 °C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Life Support Note:
Not Intended for Use in Life Support or Life Saving Applications
The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC} , I_{IN} to GND (Refer to Figure 5)	± 8, 100 µs	A
Peak Pulse Current, 8/20µs	± 14	A
ESD Ratings and Capability (Figure 1, Table 1) Load Dump and Reverse Battery (Note 2)		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
SOIC Package	170	°C/W
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s) (SOIC - Lead Tips Only)	260	°C

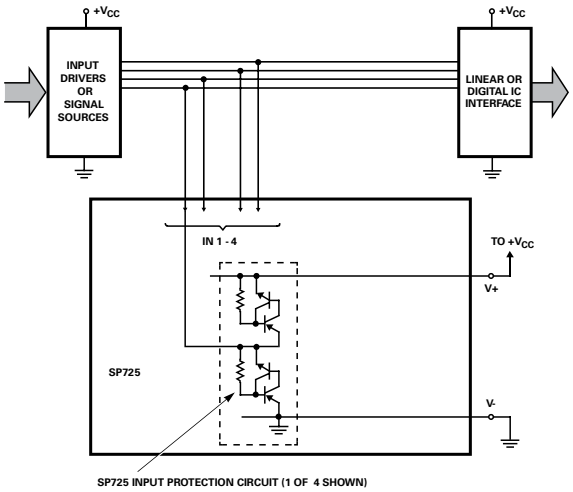
Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop IN to V-	V_{FWDL}	I_{IN} = 2A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		(Note 3)	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} ; (Note 3)	-	0.5	-	Ω
Input Capacitance	C_{IN}			5	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

Notes:
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air
2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP725 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance." These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

Typical Application of the SP725

(Application as an Input Clamp for Overvoltage, Greater than 1V_{BE} Above V+ or less than -1V_{BE} below V-)



ESD Capability

ESD capability is dependent on the application and defined test standard.The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

The SP725 has a Level 4 HBM capability when tested as a device to the IEC 61000-4-2 standard. Level 4 specifies a required capability greater than 8kV for direct discharge and greater than 15kV for air discharge.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "incircuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP725 ESD capability is typically greater than 25kV from 100pF through 1.5kΩ . By strict definition of MIL-STD-3015.7 using "pinto-pin" device testing, the ESD voltage capability is greater than 10kV.

For the SP725 EIAJ IC121 Machine Model (MM) standard, the ESD capability is typically greater than 2kV from 200pF with no series resistance.

Figure 1: Electrostatic Discharge Test

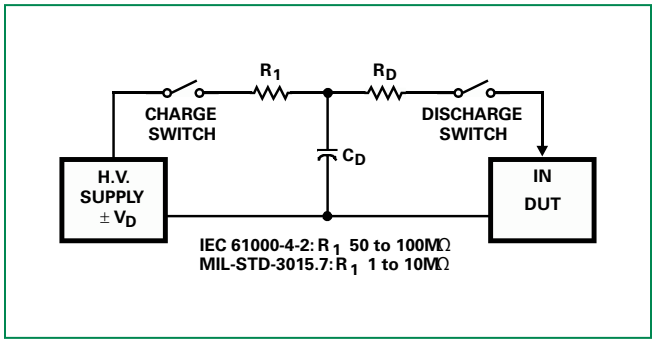


Table 1: ESD Test Conditions

Standard	Type/Mode	R_D	C_D	$\pm V_D$
IEC 61000-4-2 (Level 4)	HBM, Air Discharge	330 Ω	150pF	15kV
	HBM, Direct Discharge	330 Ω	150pF	8kV
MIL-STD-3015.7	Modified HBM	1.5k Ω	100pF	25kV
	Standard HBM	1.5k Ω	100pF	10kV
EIAJ IC121	Machine Model	0k Ω	200pF	2kV

Figure 2: Low Current SCR Forward Voltage Drop Curve

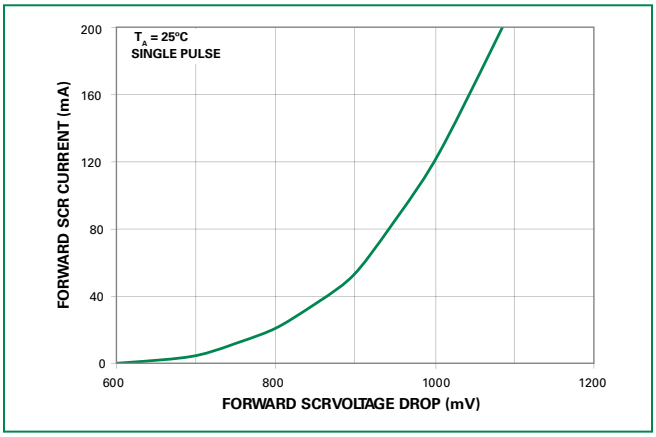
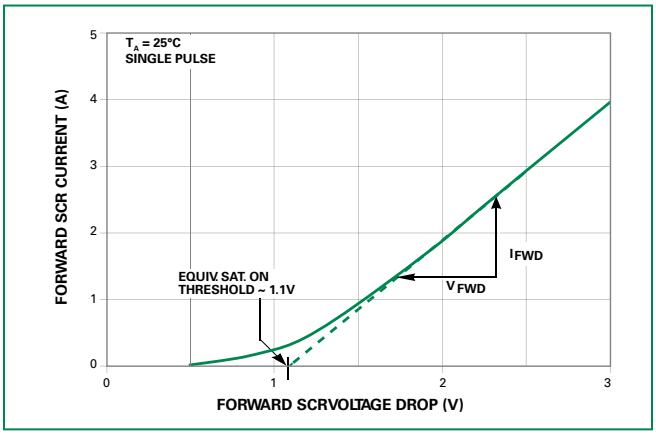


Figure 3: High Current SCR Forward Voltage Drop Curve



Peak Transient Current Capability for Long Duration Surges

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP725 's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 4.

The test circuit of Figure 4 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP725 'IN' input pin and the (+) current pulse input goes to the SP725 V- pin. The V+ to V- supply of the SP725 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 5 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25 ° C and 105 ° C and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 5.

Note that adjacent input pins of the SP725 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

Figure 4: Typical SP725 Peak Current Test Circuit with a Variable Pulse Width Input

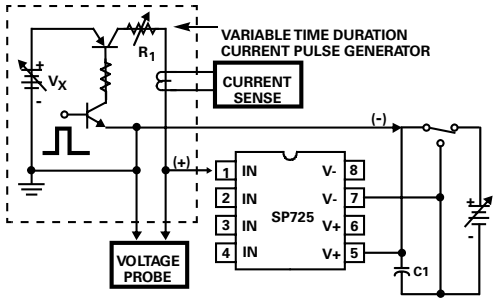
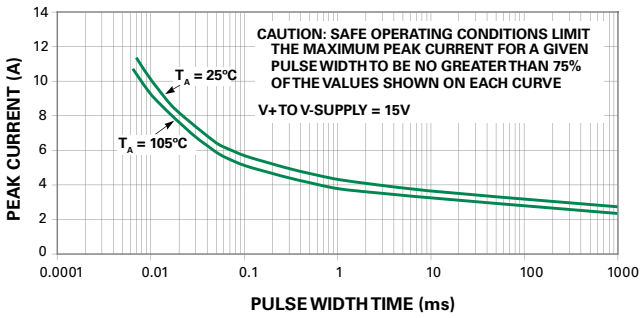


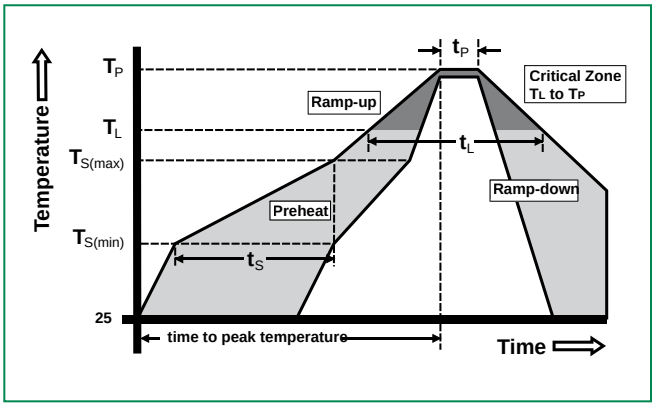
Figure 5: SP725 Typical Nonrepetitive Peak Current Pulse Capability

Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds

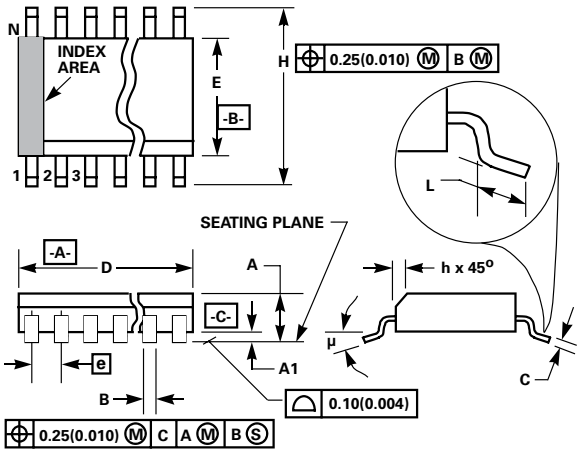


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — Small Outline Plastic Packages (SOIC)

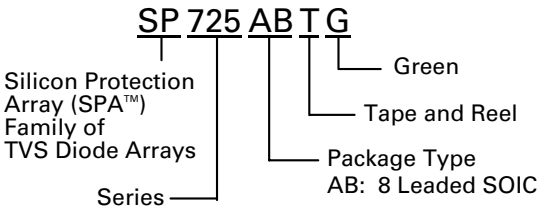


Package	SOIC				
Pins	8				
JEDEC	M8.15 MS-012-AA Issue C				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	1.35	1.75	0.0532	0.0688	-
A1	0.10	0.25	0.0040	0.0098	-
B	0.33	0.51	0.013	0.020	9
C	0.19	0.25	0.0075	0.0098	-
D	4.80	5.00	0.1890	0.1968	3
E	3.80	4.00	0.1497	0.1574	4
e	1.27 BSC		0.050 BSC		-
H	5.80	6.20	0.2284	0.2440	-
h	0.25	0.50	0.0099	0.0196	5
L	0.40	1.27	0.016	0.050	6
N	8		8		7
μ	0°	8°	0°	8°	-

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System



Product Characteristics

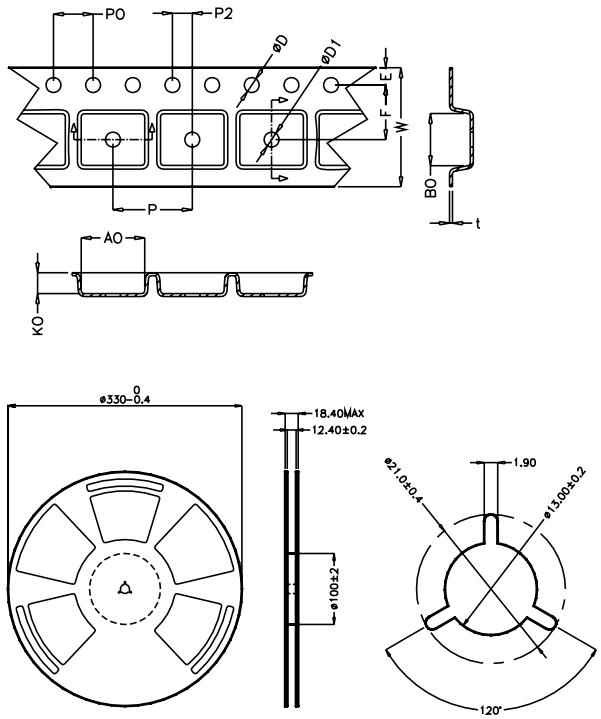
Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes:
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 ISSUE A.
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Temp. Range (°C)	Package	Marking	Min. Order Qty.
SP725ABG	-40 to 105	8 Ld SOIC	SP725AG	1960
SP725ABTG	-40 to 105	8 Ld SOIC Tape and Reel	SP725AG	2500

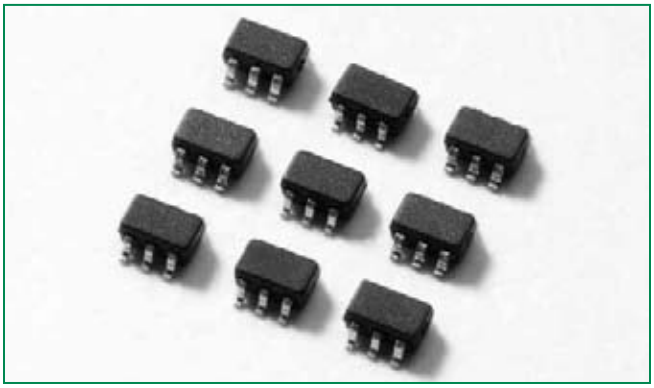
Embossed Carrier Tape & Reel Specification - SOIC Package



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

SP3001 Series 0.65pF Rail Clamp Array

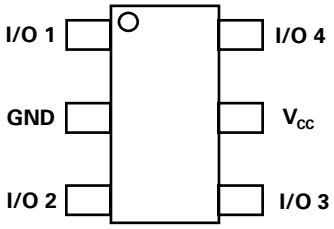
HF RoHS GREEN



Description

The SP3001 has ultra low capacitance rail-to rail diodes with an additional zener diode fabricated in a proprietary silicon avalanche technology to protect each I/O pin providing a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high speed signal pins such as HDMI, DVI, USB2.0, and IEEE 1394.

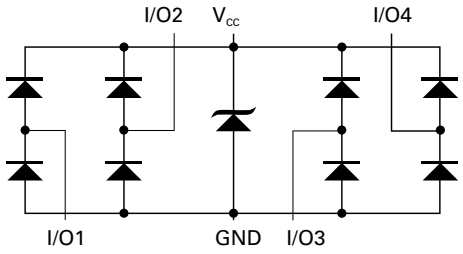
Pinout



Features

- Low capacitance of 0.65pF (TYP) per I/O
- ESD protection of ±8kV contact discharge, ±15kV air discharge, (IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small SC70 package saves board space
- Lightning Protection, IEC61000-4-5, 2.5A (8/20µs)

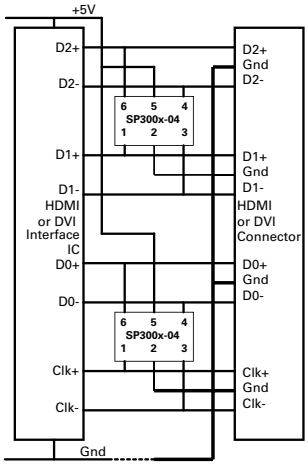
Functional Block Diagram



Applications

- Computer Peripherals
- Mobile Phones
- PDA's
- Digital Cameras
- Network Hardware/Ports
- Test Equipment
- Medical Equipment

Application Example



A single 4 channel SP300x-04 device can be used to protect four of the data lines in a HDMI/DVI interface. Two (2) SP300x-04 devices provide protection for the main data lines. Low voltage ASIC HDMI/DVI drivers can also be protected with the SP300x-04, the $+V_{CC}$ pins on the SP300x-04 can be substituted with a suitable bypass capacitor or in some backdrive applications the $+V_{CC}$ of the SP300x-04 can be floated or NC.

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	2.5	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

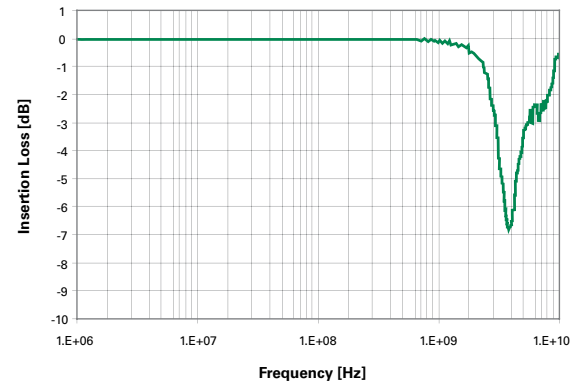
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

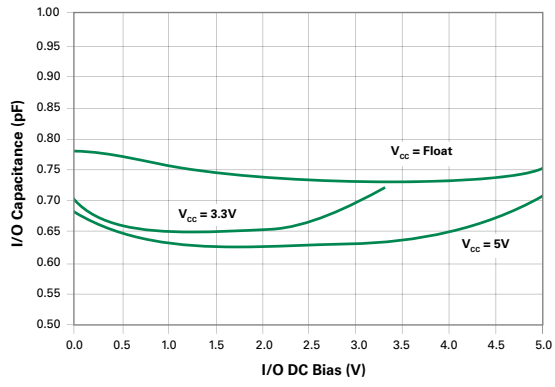
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			6	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		9.5	11.0	V
		I_{PP}=2A, t_p=8/20µs, Fwd		10.6	13.0	V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V	0.7	0.8	0.9	pF
		Reverse Bias=1.65V	0.55	0.65	0.75	pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		0.35		pF

Note: 1. Parameter is guaranteed by design and/or device characterization.

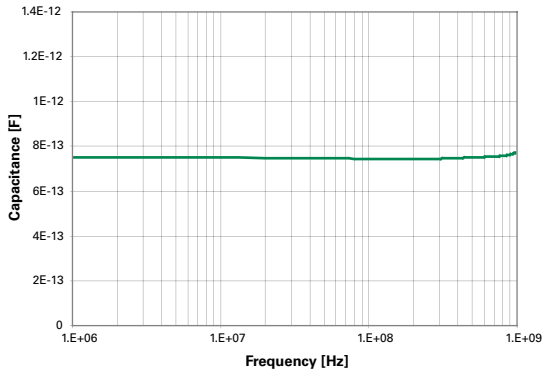
Insertion Loss (S21) I/O to GND



Capacitance vs. Bias Voltage



Capacitance vs. Frequency



Product Characteristics

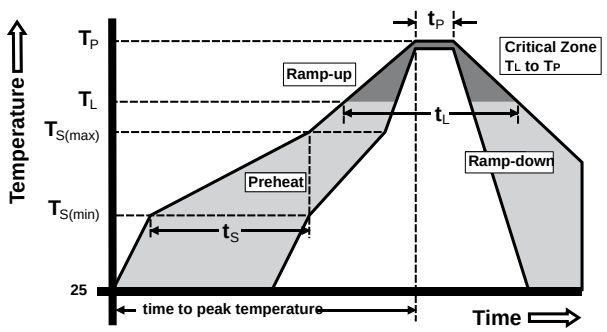
Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

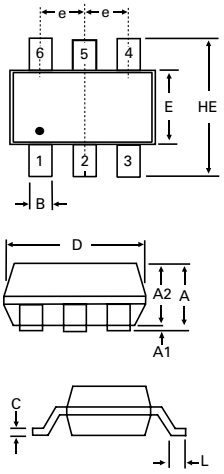
SP3001

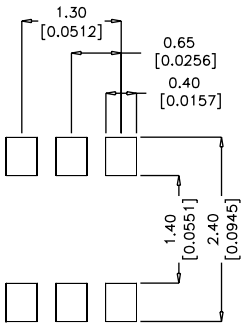
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_P)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — SC70-6

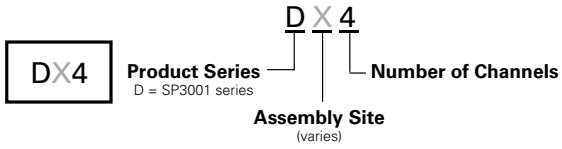




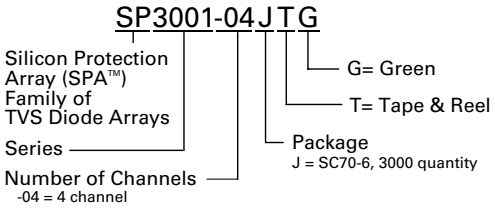
Solder Pad Layout

Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Part Marking System



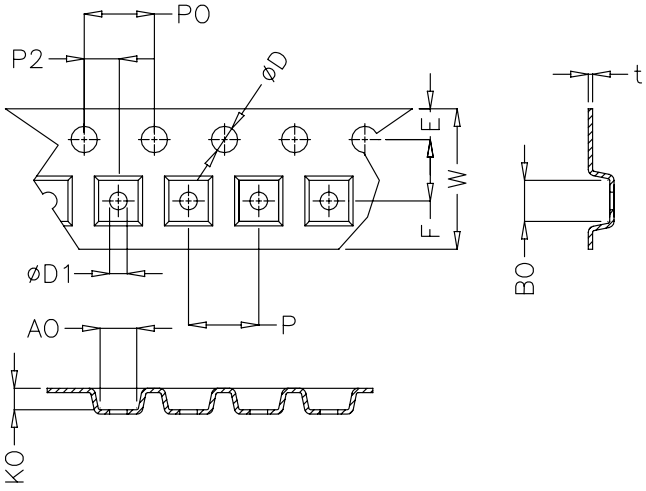
Part Numbering System



Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3001-04JTG	SC70-6	DX4	3000

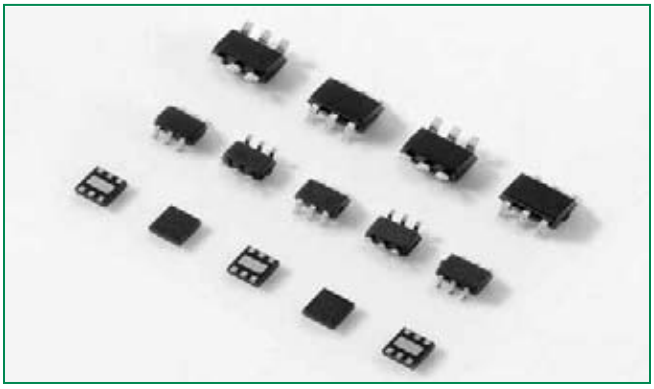
Embossed Carrier Tape & Reel Specification — SC70-6



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.072
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.076	0.081
D	1.40	1.60	0.055	0.062
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.153	0.161
10P0	40.0+/- 0.20		1.574+/-0.007	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.960
K0	1.12	1.32	0.044	0.052
t	0.27 max		0.010 max	

SP3002 Series 0.85pF Rail Clamp Array

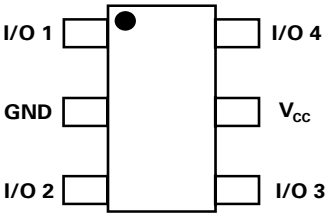
HF RoHS GREEN



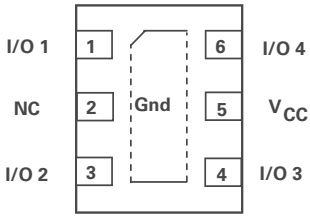
Description

The SP3002 has ultra low capacitance rail-to-rail diodes with an additional zener diode fabricated in a proprietary silicon avalanche technology to protect each I/O pin providing a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level (Level 4) specified in the IEC 61000-4-2 international standard without performance degradation. Their very low loading capacitance also makes them ideal for protecting high speed signal pins such as HDMI, DVI, USB2.0, and IEEE 1394.

Pinout



SC70-6 and SOT23-6

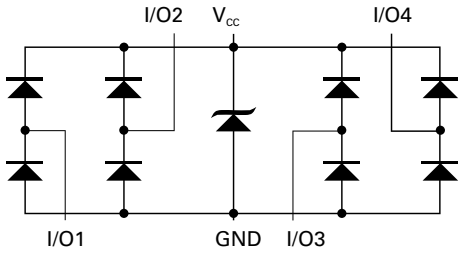


uDFN-6
(1.6x1.6x0.5mm)

Features

- Low capacitance of 0.85 pF (TYP) per I/O
- ESD protection of ±12kV contact discharge, ±15kV air discharge, (IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small packaging options saves board space
- Lightning Protection, IEC61000-4-5, 4.5A (8/20µs)

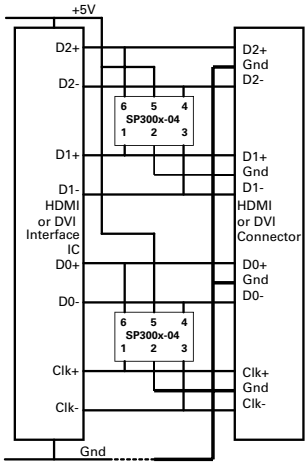
Functional Block Diagram



Applications

- Computer Peripherals
- Mobile Phones
- PDA's
- Digital Cameras
- Network Hardware/Ports
- Test Equipment
- Medical Equipment

Application Example



A single 4 channel SP300x-04 device can be used to protect four of the data lines in a HDMI/DVI interface. Two (2) SP300x-04 devices provide protection for the main data lines. Low voltage ASIC HDMI/DVI drivers can also be protected with the SP300x-04, the $+V_{CC}$ pins on the SP300x-04 can be substituted with a suitable bypass capacitor or in some backdrive applications the $+V_{CC}$ of the SP300x-04 can be floated or NC.

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	4.5	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

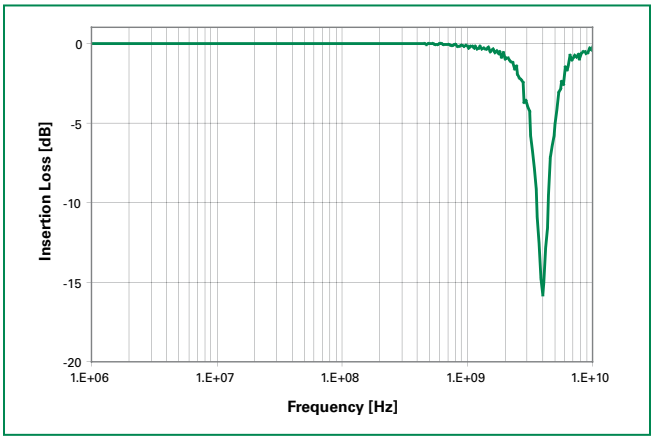
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

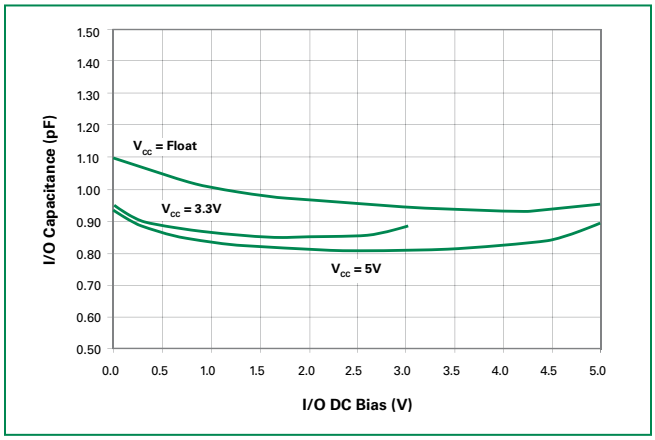
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			6.0	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		9.5	11.0	V
		I_{PP}=2A, t_p=8/20µs, Fwd		10.6	13.0	V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±12			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V	0.95	1.1	1.25	pF
		Reverse Bias=1.65V	0.7	0.85	1.0	pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		0.5		pF

Note: 1. Parameter is guaranteed by design and/or device characterization.

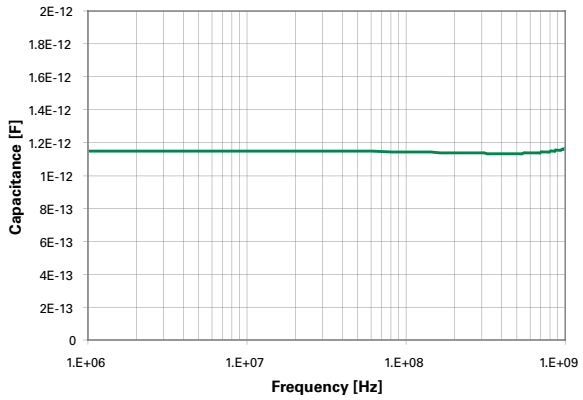
Insertion Loss (S21) I/O to GND



Capacitance vs. Bias Voltage



Capacitance vs. Frequency



Product Characteristics

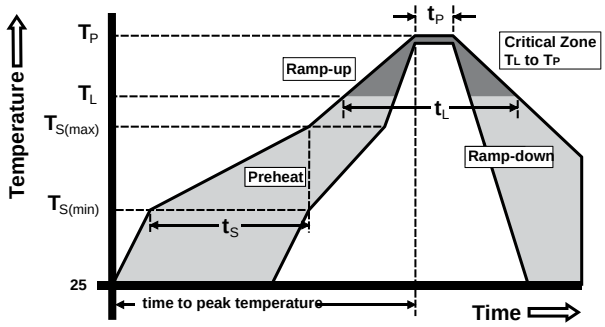
Lead Plating	SC70 & SOT23: Matte Tin uDFN: Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

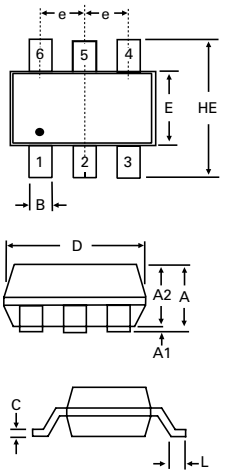
SP3002

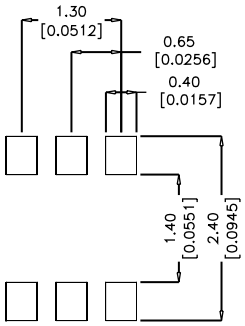
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — SC70-6

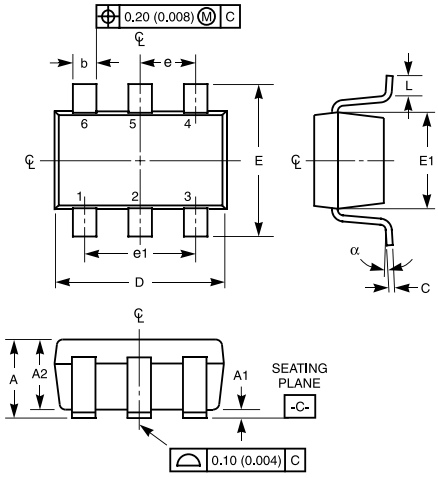




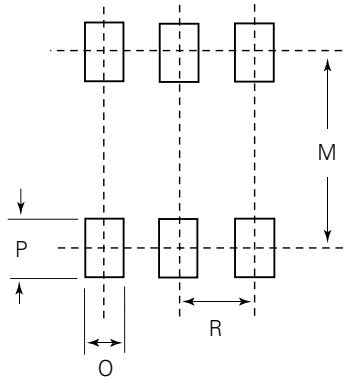
Solder Pad Layout

Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions — SOT23-6



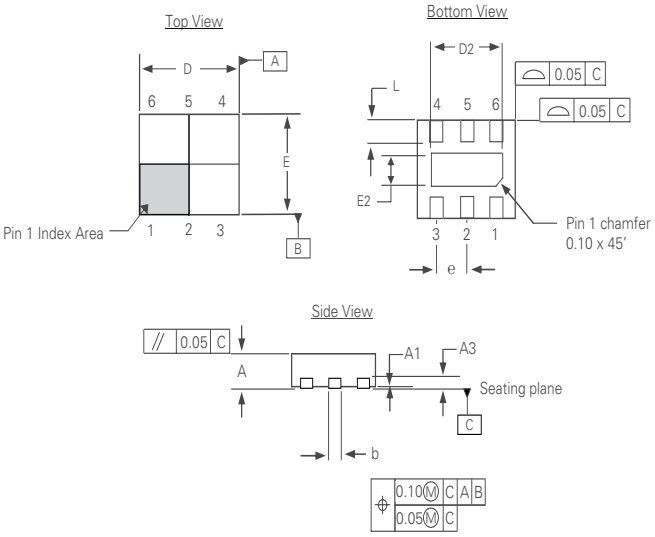
Recommended Solder Pad Layout



Package	SOT23-6				
Pins	6				
JEDEC	MO-203 Issue A				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	0.900	1.450	0.035	0.057	-
A1	0.000	0.150	0.000	0.006	-
A2	0.900	1.300	0.035	0.051	-
b	0.350	0.500	0.0138	0.0196	-
C	0.080	0.220	0.0031	0.009	-
D	2.800	3.000	0.11	0.118	3
E	2.600	3.000	0.102	0.118	-
E1	1.500	1.750	0.06	0.069	3
e	0.95 Ref		0.0374 Ref		-
e1	1.9 Ref		0.0748 Ref		-
L	0.100	0.600	0.004	0.023	4,5
N	6		6		6
a	0°	10°	0°	10°	-
M		2.590		0.102	-
O		0.690		.027 TYP	-
P		0.990		.039 TYP	-
R		0.950		0.038	-

Notes:
1. Dimensioning and tolerances per ANSI 14.5M-1982.
2. Package conforms to EIAJ SC-74 (1992).
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlenth L measured at reference to seating plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Package Dimensions — uDFN (1.6x1.6x0.5mm)



Symbol	uDFN (1.6x1.6x0.5mm)			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
A3	0.127 Ref		0.005 Ref	
b	0.20	0.30	0.008	0.012
D	1.50	1.70	0.060	0.067
D2	1.05	1.30	0.042	0.052
E	1.50	1.70	0.060	0.067
E2	0.40	0.65	0.016	0.026
e	0.50 Ref		0.020 Ref	
L	0.25	0.40	0.010	0.016

Part Numbering System

SP3002-04XTG

- SP3002 — Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- -04 — Series; Number of Channels (-04 = 4 channel)
- X — Package: H= SOT23-6, J = SC70-6, U= uDFN-6
- T — T= Tape & Reel
- G — G= Green

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3002-04HTG	SOT23-6	EX4	3000
SP3002-04JTG	SC70-6	EX4	3000
SP3002-04UTG	uDFN-6 (1.6x1.6x0.5mm)	EX4	3000

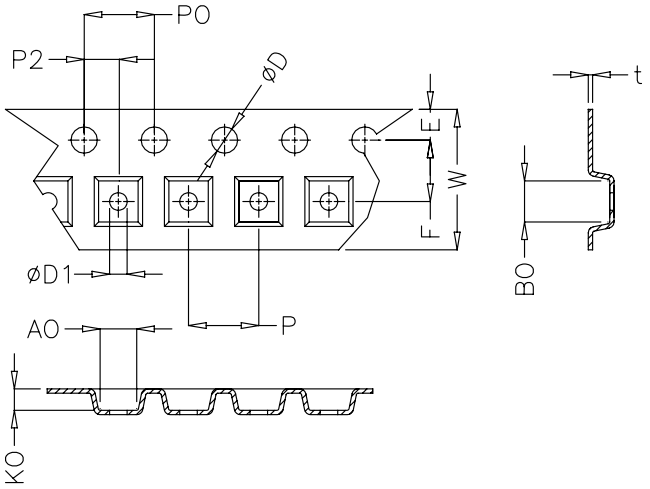
Part Marking System

EX4

E X 4

- E — **Product Series**: E = SP3002 series
- X — **Assembly Site** (varies)
- 4 — **Number of Channels**

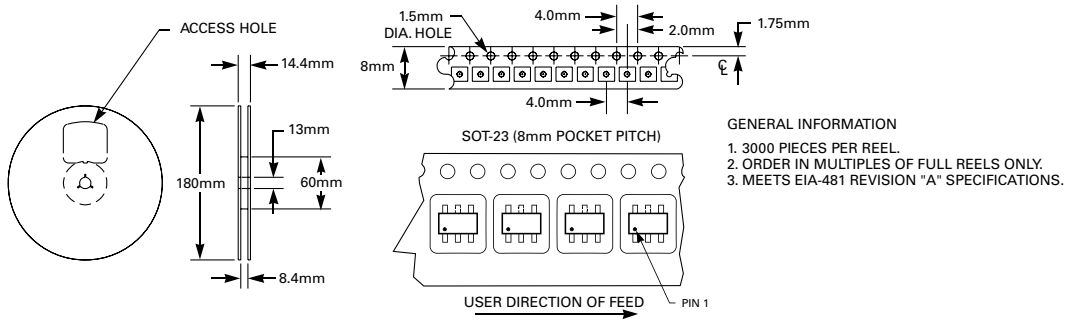
Embossed Carrier Tape & Reel Specification — SC70-6



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0+/- 0.20		1.574+/-0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.096
K0	1.12	1.32	0.044	0.052
t	0.27 Max		0.010 Max	

Embossed Carrier Tape & Reel Specification — SOT23-6

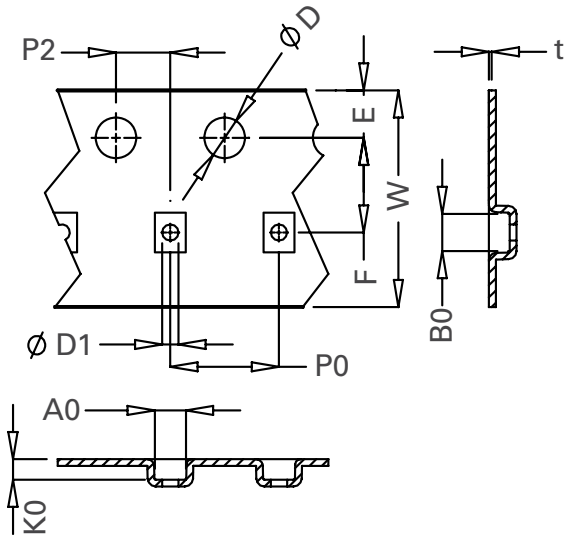
8mm TAPE AND REEL



GENERAL INFORMATION

1. 3000 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

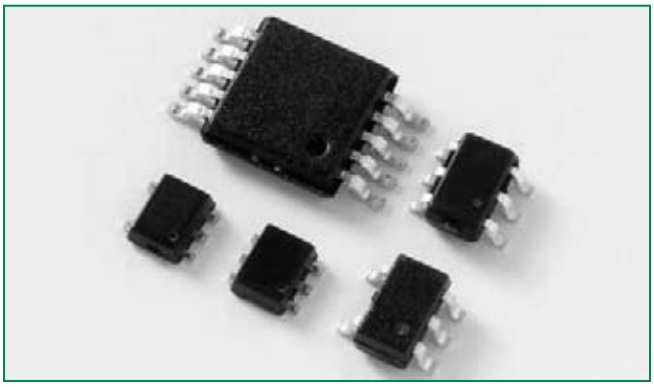
Embossed Carrier Tape & Reel Specification — uDFN-6 (1.6x1.6x0.5mm)



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.06	0.07
F	3.45	3.55	0.14	0.14
D1	1.00	1.25	0.04	0.05
D	1.50 MIN		0.06 MIN	
P0	3.90	4.10	0.15	0.16
10P0	40.0+/- 0.20		1.57+/-0.01	
W	7.90	8.30	0.31	0.33
P2	1.95	2.05	0.08	0.08
A0	1.78	1.88	0.07	0.07
B0	1.78	1.88	0.07	0.07
K0	0.84	0.94	0.03	0.04
t	0.25 TYP		0.01 TYP	

SP3003 Series 0.65pF Rail Clamp Array

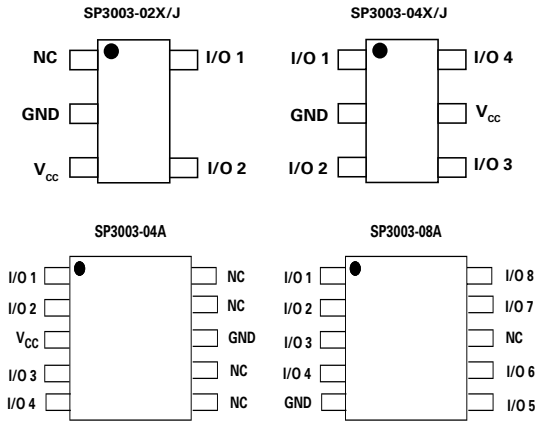
HF RoHS GREEN



Description

The SP3003 has ultra low capacitance rail-to-rail diodes with an additional zener diode fabricated in a proprietary silicon avalanche technology to protect each I/O pin providing a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high speed signal pins such as HDMI, DVI, USB2.0, and IEEE 1394.

Pinout



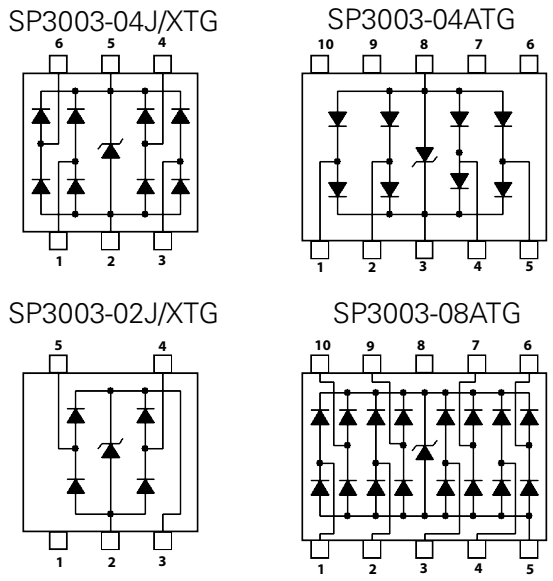
Features

- ESD protection of ±8kV contact discharge, ±15kV air discharge, (IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50ns)
- Lightning Protection, IEC61000-4-5, 2.5A (8/20µs)
- Low capacitance of 0.65pF (TYP) per I/O
- Low leakage current of 0.5µA (MAX) at 5V
- Complete line of small packaging helps save board space (SC70, SOT553, SOT563, MSOP10)

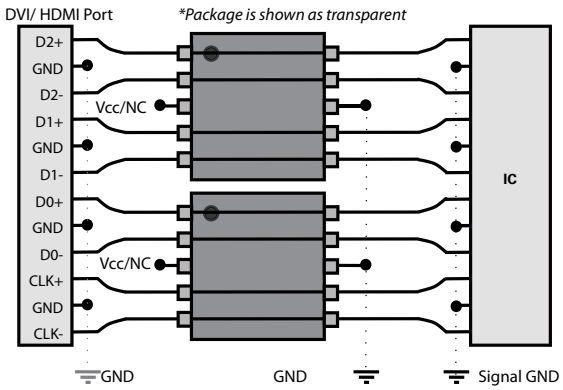
Applications

- LCD/ PDP TVs
- DVD Players
- Desktops
- MP3/ PMP
- Digital Cameras
- Set Top Boxes
- Mobile Phones
- Notebooks
- Computer Peripherals

Functional Block Diagram



Application Example



A single, 4 channel SP3003-04 device can be used to protect four (4) of the data lines in a HDMI/DVI interface so two (2) SP3003-04 devices provide protection for all eight (8) TMDS lines.

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	2.5	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

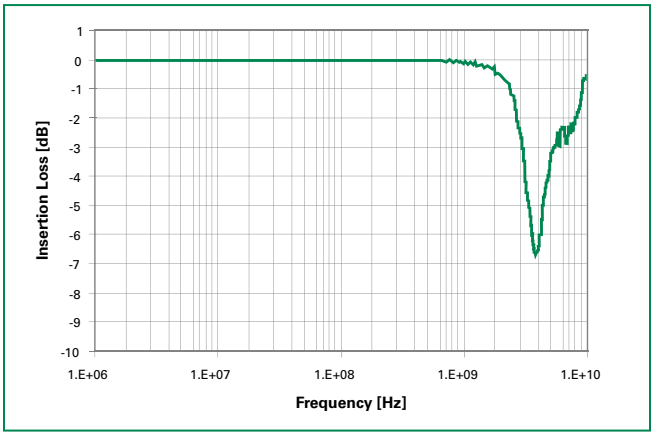
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

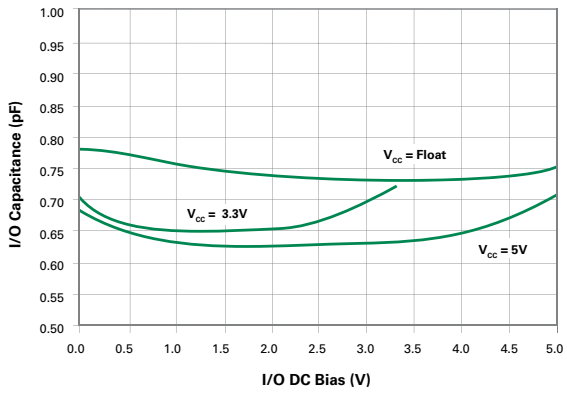
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			6	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		10.0	12.0	V
		I_{PP}=2A, t_p=8/20µs, Fwd		11.8	15.0	V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V	0.7	0.8	0.95	pF
		Reverse Bias=1.65V	0.55	0.65	0.8	pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		0.35		pF

Note: 1. Parameter is guaranteed by design and/or device characterization.

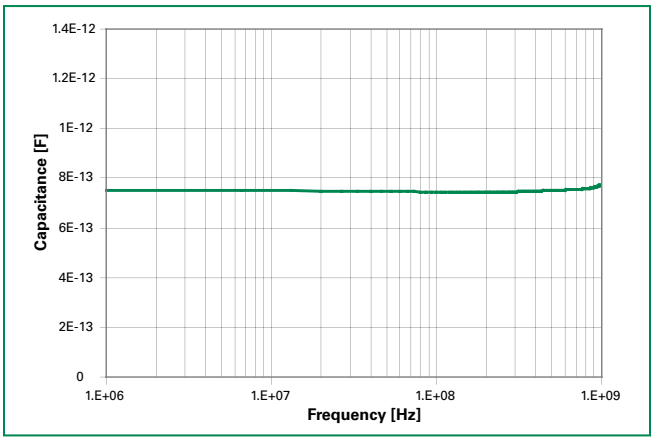
Insertion Loss (S21) I/O to GND



Capacitance vs. Bias Voltage



Capacitance vs. Frequency



Product Characteristics

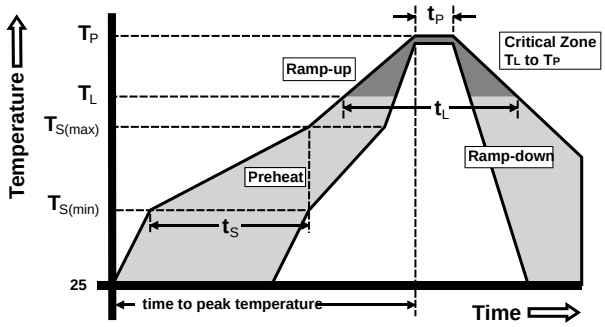
Lead Plating	Matte Tin (SC70-x, MSOP-10) Pre-Plated Frame (SOT5x3)
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

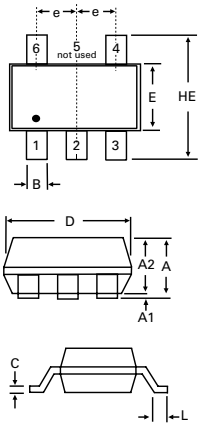
SP3003

Soldering Parameters

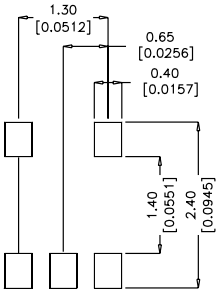
Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — SC70-5

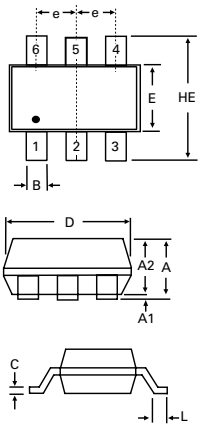


Solder Pad Layout

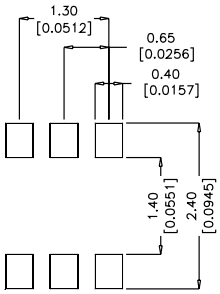


Package	SC70-5			
Pins	5			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions — SC70-6

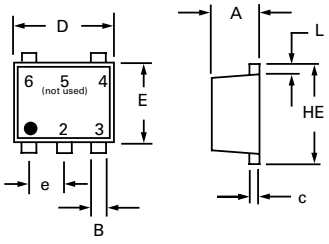


Solder Pad Layout

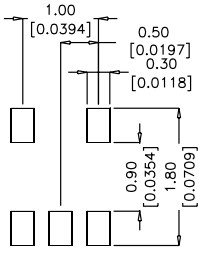


Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions — SOT553

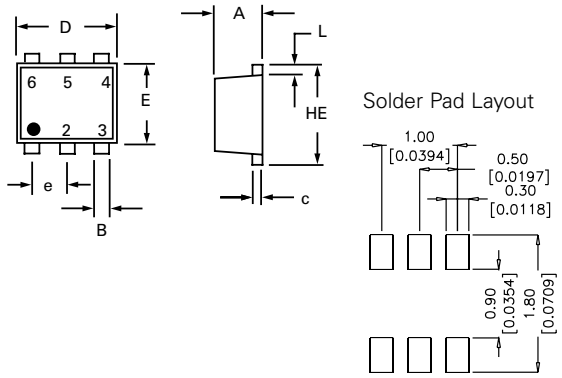


Solder Pad Layout



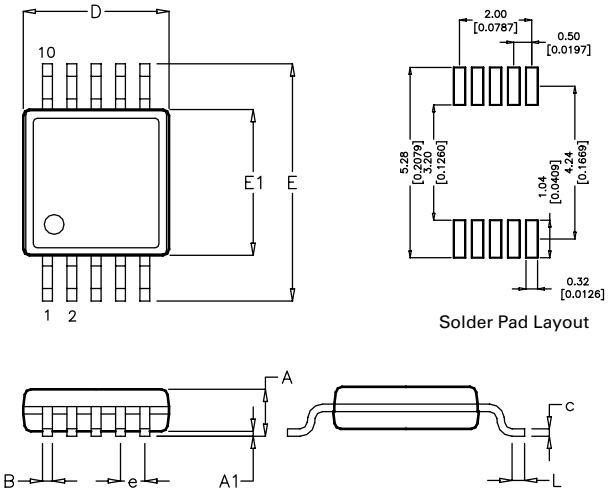
Package	SOT 553			
Pins	5			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

Package Dimensions — SOT563



Package	SOT 563			
Pins	6			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

Package Dimensions — MSOP10



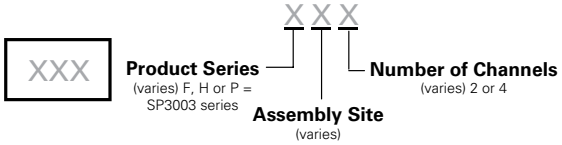
Package	MSOP10			
Pins	10			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.10	-	0.043
A1	0.00	0.15	0.000	0.006
B	0.17	0.27	0.007	0.011
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.67	5.10	0.184	0.200
E1	2.90	3.10	0.114	0.122
e	0.50 BSC		0.020 BSC	
HE	0.40	0.80	0.016	0.031

Part Numbering System

SP3003-0X XTG

- Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- Series
- Number of Channels
  - -02 = 2 channel (SC70-5, SOT553 packages)
  - -04 = 4 channel (SC70-6, SOT563, MSOP-10 packages)
  - -08 = 8 channel (MSOP-10 packages)
- Package
  - A = MSOP-10, 4000 quantity
  - J = SC70-5 or SC70-6, 3000 quantity
  - X = SOT553 or SOT563, 5000 quantity
- T= Tape & Reel
- G= Green

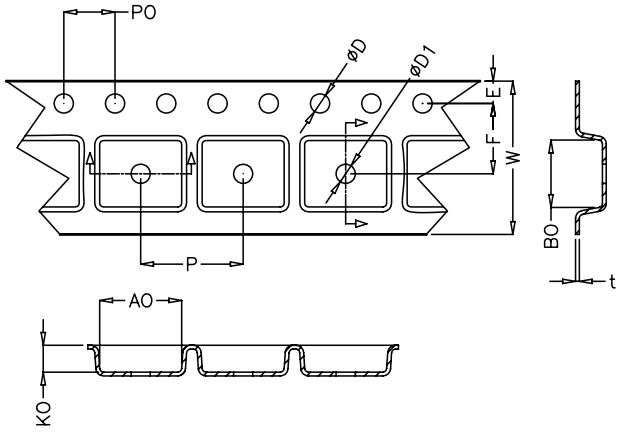
Part Marking System



Ordering Information

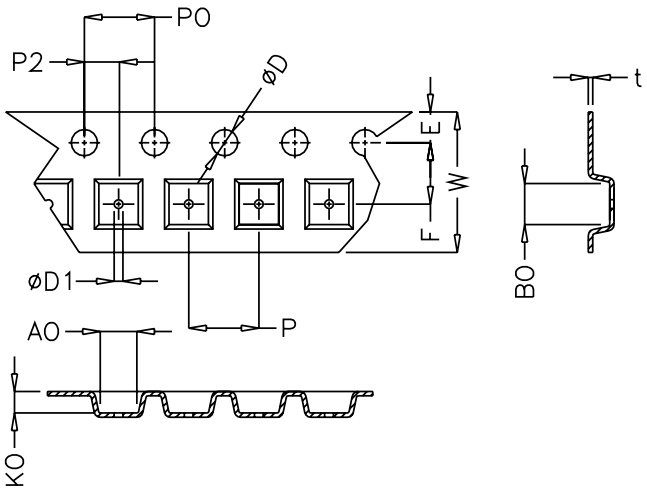
Part Number	Package	Marking	Min. Order Qty.
SP3003-02JTG	SC70-5	HX2	3000
SP3003-02XTG	SOT553	HX2	5000
SP3003-04ATG	MSOP-10	FX4	4000
SP3003-04JTG	SC70-6	FX4	3000
SP3003-04XTG	SOT563	FX4	5000
SP3003-08ATG	MSOP-10	FX8	4000

Embossed Carrier Tape & Reel Specification — MSOP-10



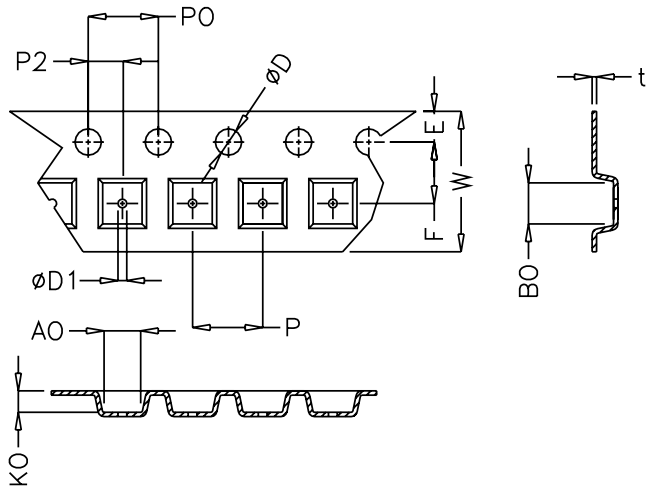
	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.40	5.60	0.213	0.220
D	1.50	1.60	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.90	4.10	0.154	0.161
10P0	40.0+/- 0.20		1.574+/-0.008	
W	11.90	12.10	0.469	0.476
P	7.90	8.10	0.311	0.319
A0	5.20	5.40	0.205	0.213
B0	3.20	3.40	0.126	0.134
K0	1.20	1.40	0.047	0.055
t	0.30 +/- 0.05		0.012+/- 0.002	

Embossed Carrier Tape & Reel Specifications — SC70-5 and SC70-6



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0+/- 0.20		1.574+/-0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.960
K0	1.12	1.32	0.044	0.052
t	0.27 max		0.010 max	

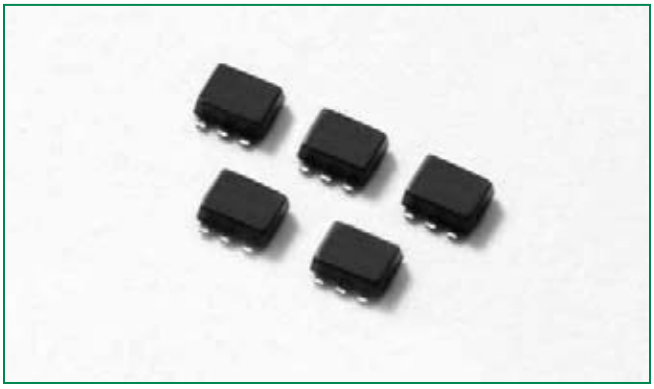
Embossed Carrier Tape & Reel Specifications — SOT553 and SOT563



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.076	0.081
D	1.40	1.60	0.055	0.063
D1	0.45	0.55	0.017	0.021
P0	3.90	4.10	0.154	0.161
10P0	40.0+/- 0.20		1.574+/-0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	1.73	1.83	0.068	0.072
B0	1.73	1.83	0.068	0.072
K0	0.64	0.74	0.025	0.029
t	0.22 max		0.009 max	

SP3004 Series 0.85pF Rail Clamp Array

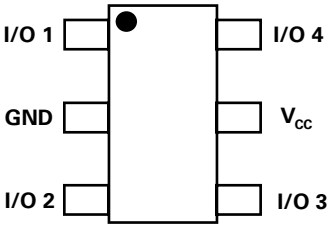
HF RoHS GREEN



Description

The SP3004 has ultra low capacitance rail-to rail diodes with an additional zener diode fabricated in a proprietary silicon avalanche technology to protect each I/O pin providing a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level (Level 4) specified in the IEC 61000-4-2 international standard without performance degradation. Their very low loading capacitance also makes them ideal for protecting high speed signal pins such as HDMI, DVI, USB2.0, and IEEE 1394.

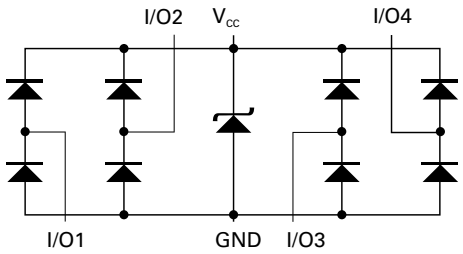
Pinout



Features

- Low capacitance of 0.85pF (TYP) per I/O
- ESD protection of ±12kV contact discharge, ±15kV air discharge, (IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small SOT563 package saves board space
- Lightning Protection, IEC61000-4-5, 4A (8/20µs)

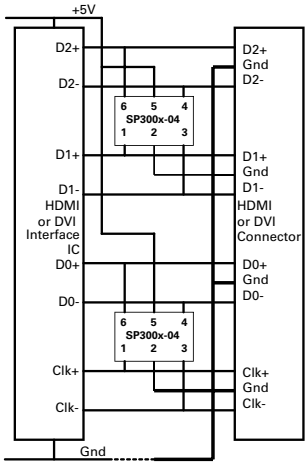
Functional Block Diagram



Applications

- Computer Peripherals
- Mobile Phones
- PDA's
- Digital Cameras
- Network Hardware/Ports
- Test Equipment
- Medical Equipment

Application Example



A single 4 channel SP300x-04 device can be used to protect four of the data lines in a HDMI/DVI interface. Two (2) SP300x-04 devices provide protection for the main data lines. Low voltage ASIC HDMI/DVI drivers can also be protected with the SP300x-04, the $+V_{CC}$ pins on the SP300x-04 can be substituted with a suitable bypass capacitor or in some backdrive applications the $+V_{CC}$ of the SP300x-04 can be floated or NC.

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	4	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

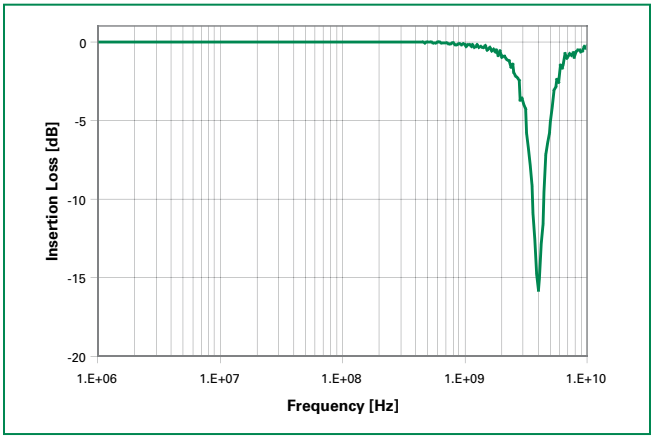
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

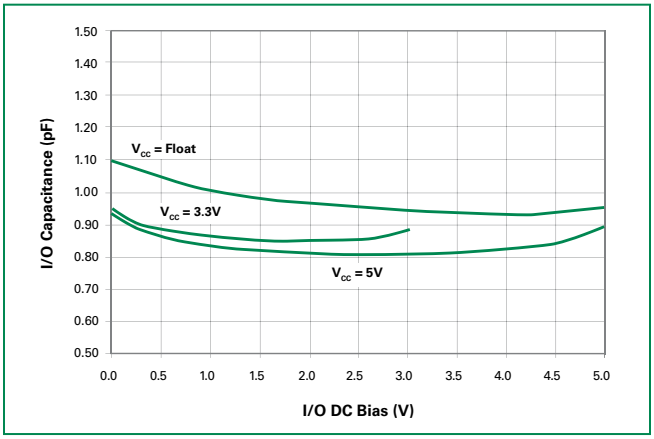
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			6	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		10.0	12.0	V
		I_{PP}=2A, t_p=8/20µs, Fwd		11.8	15.0	V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±12			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V	0.95	1.1	1.25	pF
		Reverse Bias=1.65V	0.7	0.85	1	pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		0.5		pF

Note: [1] Parameter is guaranteed by design and/or device characterization.

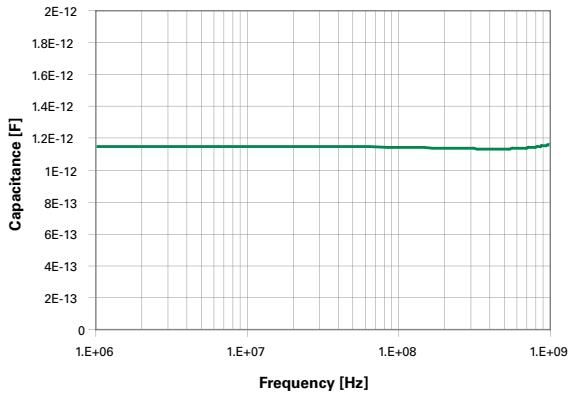
Insertion Loss (S21) I/O to GND



Capacitance vs. Bias Voltage



Capacitance vs. Frequency



Product Characteristics

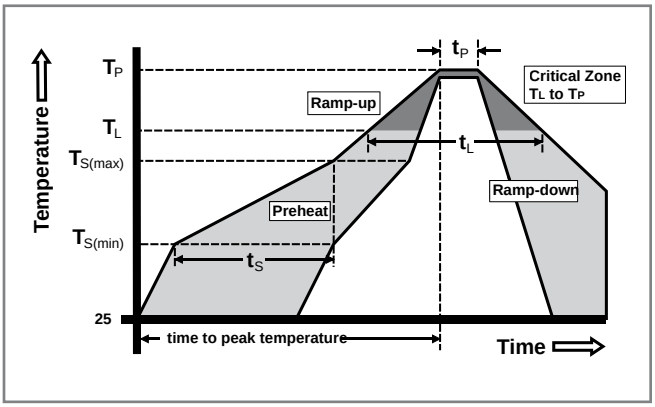
Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

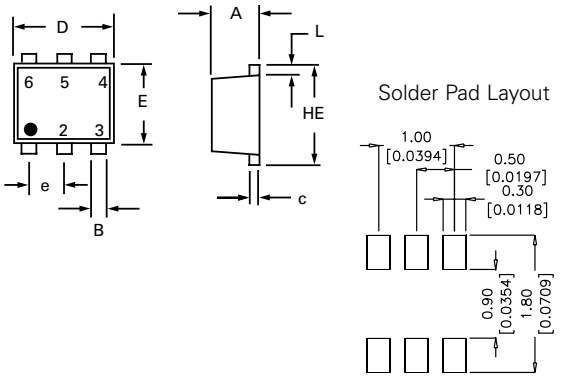
SP3004

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

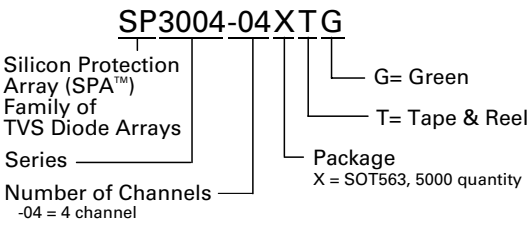


Package Dimensions — SOT563

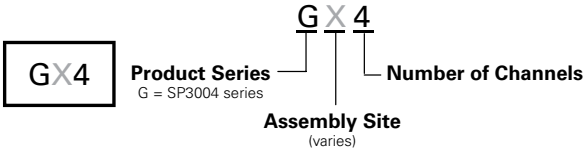


Package	SOT 563			
Pins	6			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

Part Numbering System



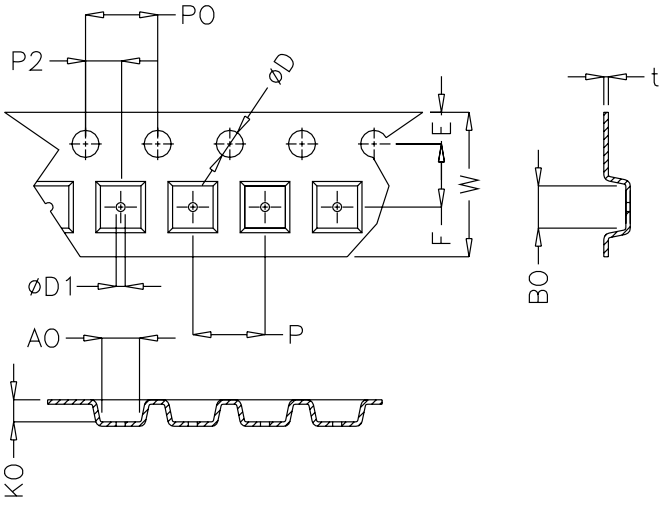
Part Marking System



Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3004-04XTG	SOT563	GX4	5000

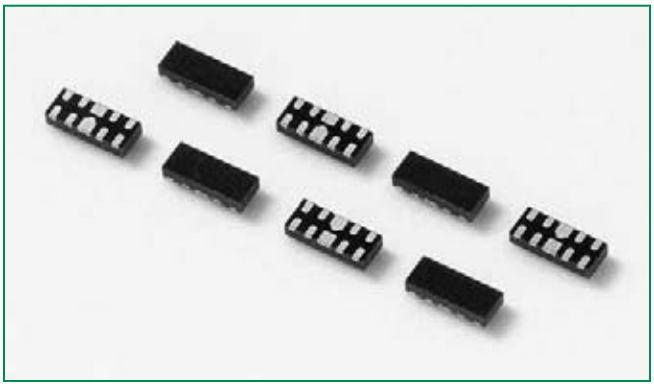
Embossed Carrier Tape & Reel Specification — SOT563



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	0.45	0.55	0.017	0.021
P0	3.90	4.10	0.154	0.161
10P0	40.0+/- 0.20		1.574+/-0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	1.73	1.83	0.068	0.072
B0	1.73	1.83	0.068	0.072
K0	0.64	0.74	0.025	0.029
t	0.22 max		0.009 max	

SP3010 Series 0.45pF Rail Clamp Array

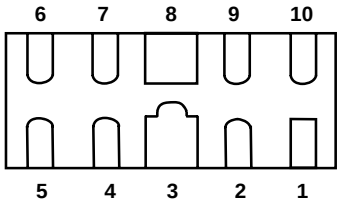
HF RoHS GREEN



Description

The SP3010 integrates 4 channels of ultra-low capacitance rail-to-rail diodes and an additional zener diode to provide protection for electronic equipment that may experience destructive electrostatic discharges (ESD). This robust device can safely absorb repetitive ESD strikes at the maximum level specified in the IEC61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. The extremely low loading capacitance also makes it ideal for protecting high speed signal pins such as HDMI, USB3.0, USB2.0, and IEEE 1394.

Pinout

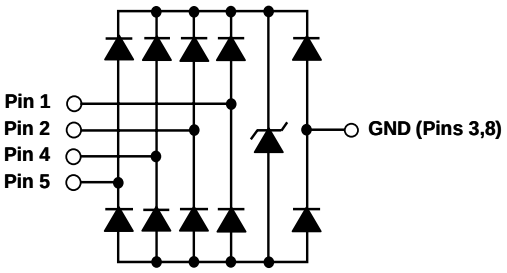


*Pins 6, 7, 9, 10 are not internally connected but should be connected to the trace.

Features

- ESD, IEC61000-4-2, ±8kV contact, ±15kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 3A (t_P=8/20μs)
- Low capacitance of 0.45pF (TYP) per I/O
- Low leakage current of 0.1μA (TYP) at 5V
- Small form factor uDFN package saves board space

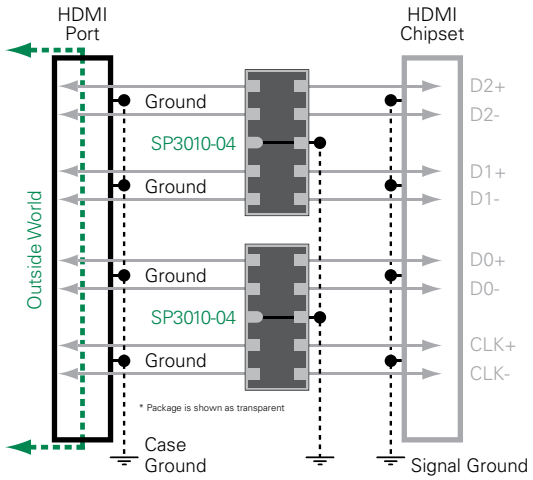
Functional Block Diagram



Applications

- LCD/PDP TVs
- DVD Players
- Desktops
- MP3/PMP
- Set Top Boxes
- Mobile Phones
- Notebooks
- Digital Cameras

Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	3.0	A
T_{OP}	Operating Temperature	-55 to 125	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

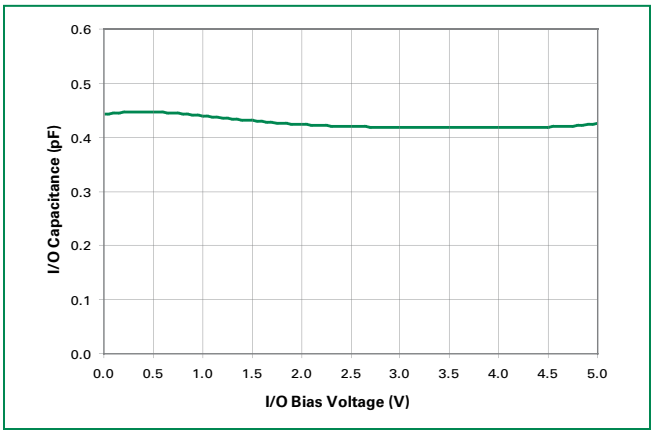
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics (T_{OP}=25°C)

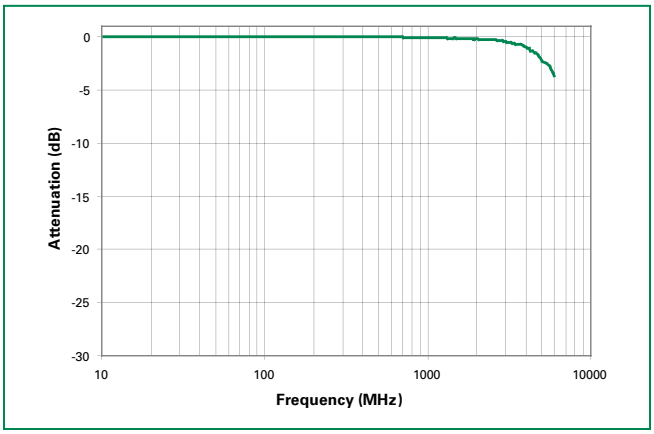
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			6.0	V
Reverse Leakage Current	I_{LEAK}	V_R=5V, Any I/O to GND		0.1	0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		10.8		V
		I_{PP}=2A, t_p=8/20µs, Fwd		12.3		V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		1.5		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V		0.45		pF

Note: [1] Parameter is guaranteed by design and/or device characterization.

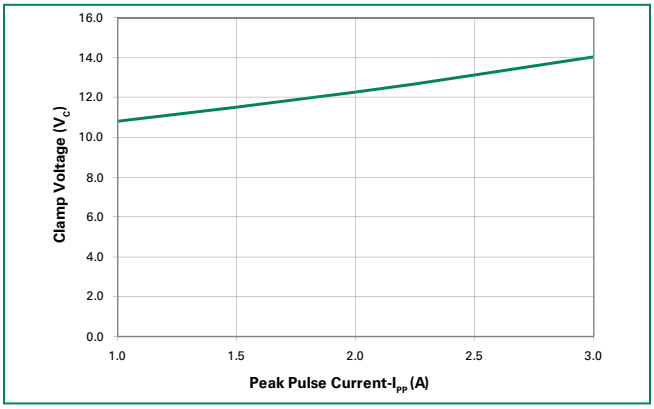
Capacitance vs. Bias Voltage



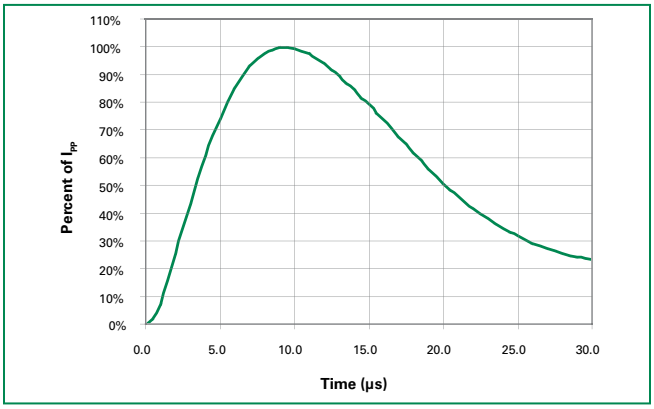
Insertion Loss (S21) I/O to GND



Clamping Voltage vs. I_{PP}

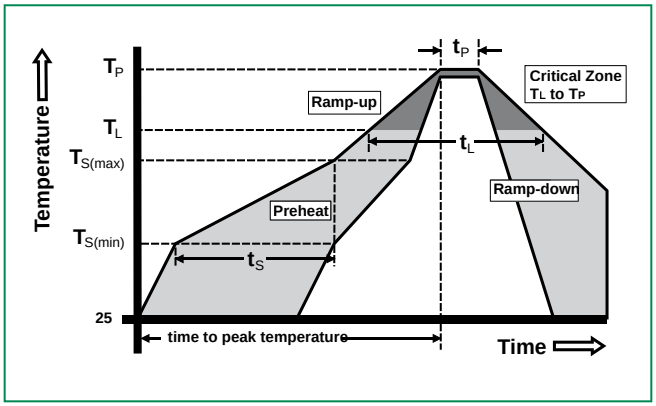


Pulse Waveform



Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Part Numbering System

SP 3010 - 0x U T G

- Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- Series
- Number of Channels
  - -04 = 4 Channel
- Package
  - UDFN-10 (2.5x1.0mm)
- T= Tape & Reel
- G= Green

Part Marking System

Q H 4

- Product Series
  - Q = SP3010
- Assembly Site
- Number of Channels

Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

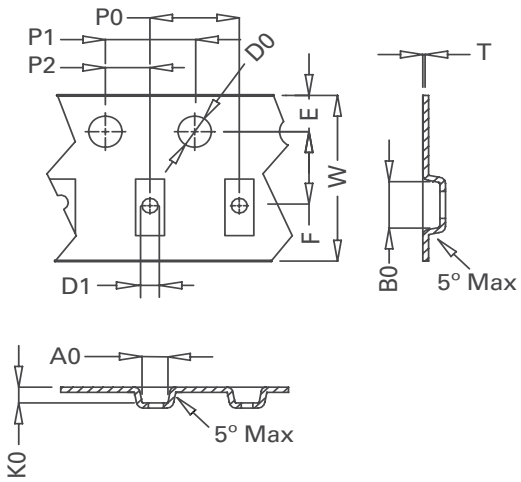
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3010-04UTG	uDFN-10	QH4	3000

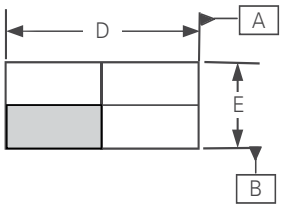
Embossed Carrier Tape & Reel Specification — UDFN-10



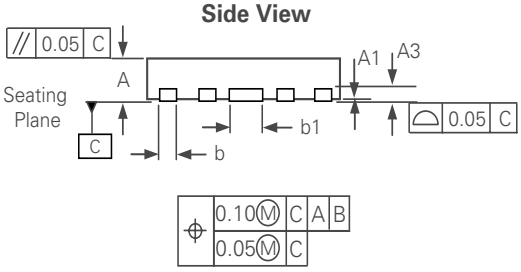
Package	uDFN-10 (2.5x1.0x0.5mm)
Symbol	Millimeters
A0	1.30 +/- 0.10
B0	2.83 +/- 0.10
D0	Ø 1.50 + 0.10
D1	Ø 1.00 + 0.25
E	1.75 +/- 0.10
F	3.50 +/- 0.05
K0	0.65 +/- 0.10
P0	4.00 +/- 0.10
P1	4.00 +/- 0.10
P2	2.00 +/- 0.05
T	0.254 +/- 0.02
W	8.00 + 0.30 /- 0.10

Package Dimensions — uDFN-10 (2.5x1.0x0.5mm)

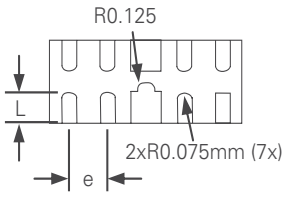
Top View



Side View



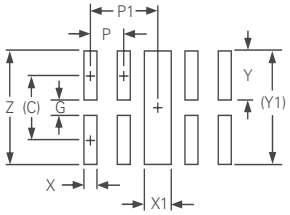
Bottom View



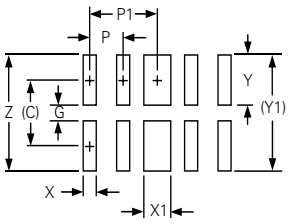
uDFN-10 (2.5x1.0x0.5mm)						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.48	0.515	0.55	0.019	0.020	0.021
A1	0.00	--	0.05	0.000		0.022
A3	0.125 Ref			0.005 Ref		
b	0.15	0.20	0.25	0.006	0.008	0.012
b1	0.35	0.40	0.45	0.014	0.016	0.018
D	2.40	2.50	2.60	0.094	0.098	0.102
E	0.90	1.00	1.10	0.035	0.039	0.043
e	0.50 BSC			0.020 BSC		
L	0.30	0.365	0.43	0.012	0.014	0.016

Soldering Pad Layout Dimensions		
	Inch	Millimeter
C	(0.034)	(0.875)
G	0.008	0.20
P	0.020	0.50
P1	0.039	1.00
X	0.008	0.20
X1	0.016	0.40
Y	0.027	0.675
Y1	(0.061)	(1.55)
Z	0.061	1.55

Recomended Soldering Pad Layout

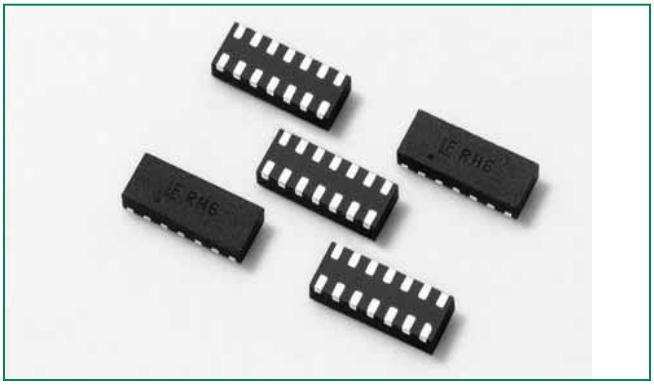


Alternative Soldering Pad Layout



SP3011 Series 0.40pF Rail Clamp Array for USB 3.0

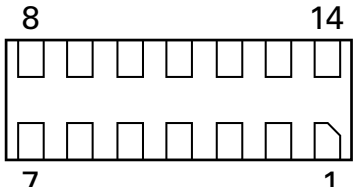
HF RoHS GREEN



Description

The SP3011 integrates six channels of ultra-low capacitance rail-to-rail diodes and an additional zener diode to provide protection for USB 3.0 ports that may experience destructive electrostatic discharges (ESD). This high density array can safely absorb repetitive ESD strikes at the maximum level specified in the IEC61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. It's extremely low loading capacitance makes it ideal for protecting any high-speed signal pins.

Pinout

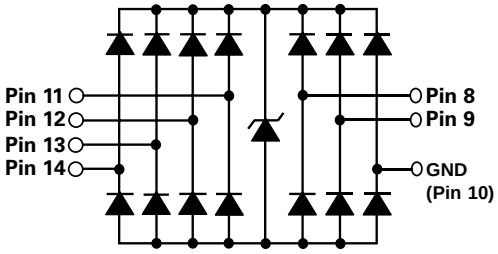


*Pins 1, 2, 3, 4, 5, 6, 7 are not internally connected but should be connected to the opposite pin with the PCB trace.

Features

- ESD, IEC61000-4-2, ±8kV contact, ±15kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 3A (8/20μs)
- Low capacitance of 0.4pF (TYP) per I/O
- Low leakage current of 0.1μA (TYP) at 5V
- Small form factor uDFN package saves board space

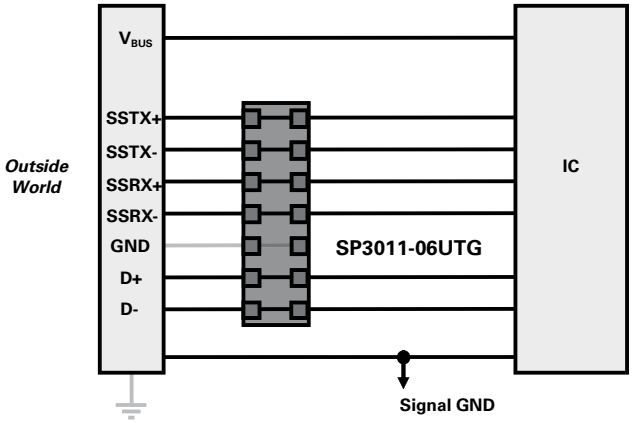
Functional Block Diagram



Applications

- Notebooks
- External Storage
- Digital Camcorder
- MP3/PMP Player
- Desktops
- Ultramobile PC
- Smartphone
- Set Top Box (DVR/PVR)

Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	3.0	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

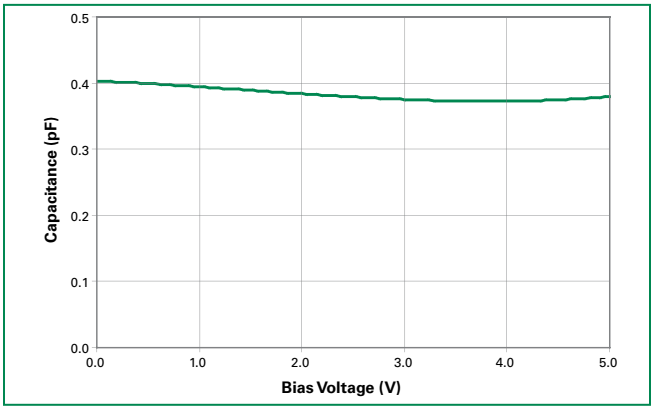
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics (T_{OP}=25°C)

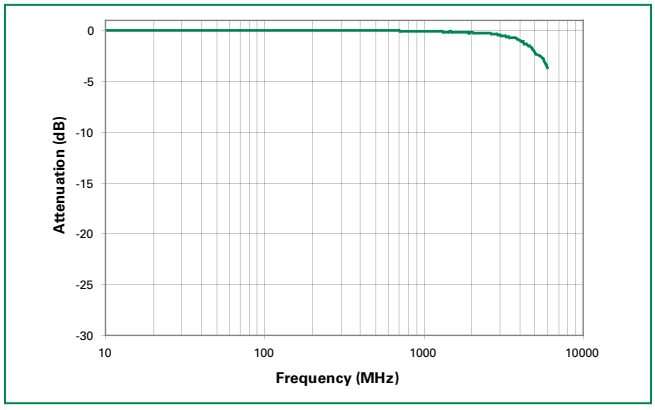
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			6.0	V
Reverse Leakage Current	I_{LEAK}	V_R=5V, Any I/O to GND		0.1	0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		11.0		V
		I_{PP}=2A, t_p=8/20µs, Fwd		12.5		V
Dynamic Resistance	R_{DYN}	$(V_{C2}-V_{C1}) / (I_{PP2}-I_{PP1})$		1.5		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V		0.4		pF

Note: [1] Parameter is guaranteed by design and/or device characterization.

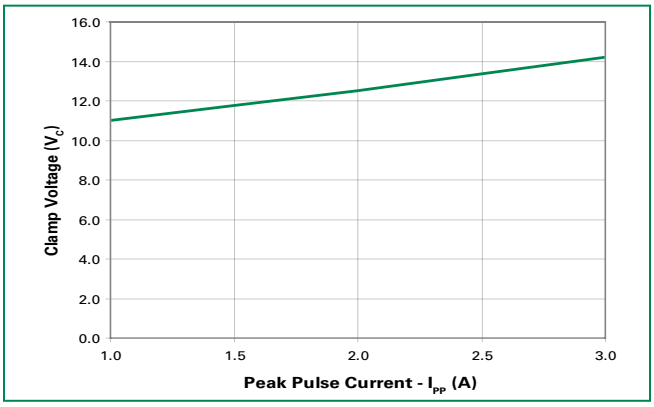
Capacitance vs. Bias Voltage



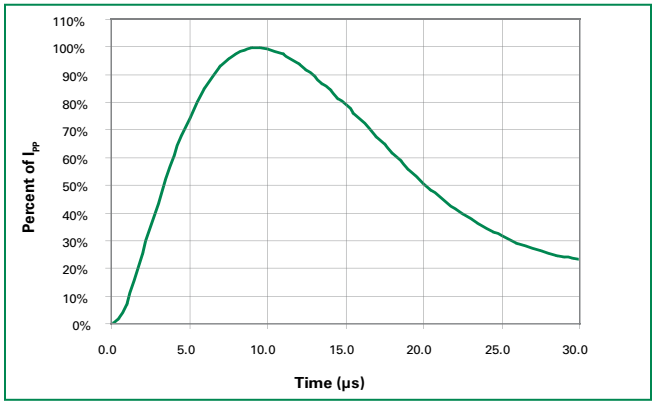
Insertion Loss (S21) I/O to GND



Clamping Voltage vs. I_{PP}

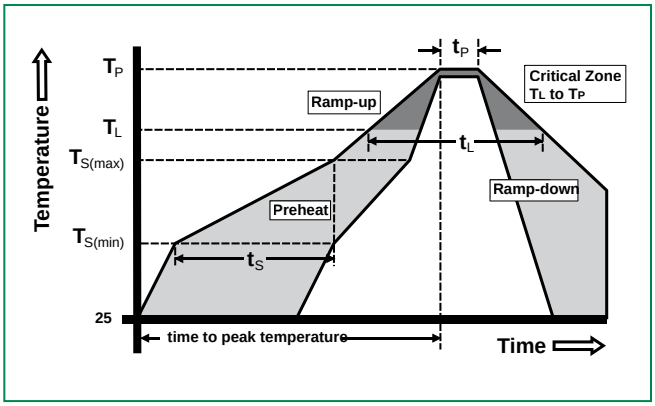


Pulse Waveform



Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Part Numbering System

SP 3011 - 06 U T G

- SP 3011: Silicon Protection Array (SPA™) Family of TVS Diode Arrays; Series
- 06: Number of Channels; -06 = 6 Channels
- U: Package; uDFN-14 (3.5x1.35mm)
- T: T= Tape & Reel
- G: G= Green

Part Marking System

R H 6

- R: Product Series; R = SP3011
- H: Assembly Site
- 6: Number of Channels

Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

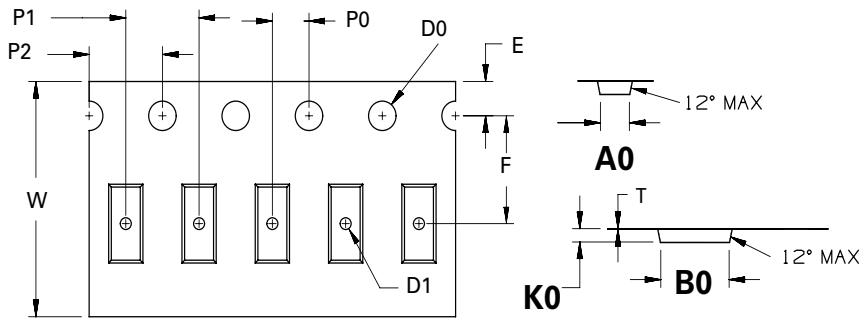
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3011-06UTG	uDFN-14	RH6	3000

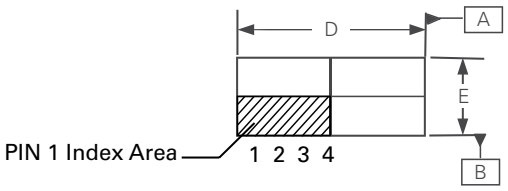
Embossed Carrier Tape & Reel Specification — uDFN-14



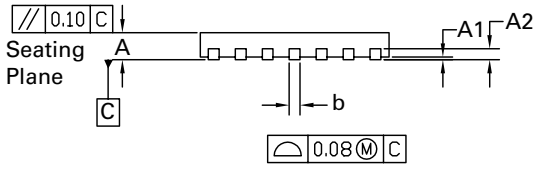
Symbol	Millimeters
A0	1.58 +/- 0.10
B0	3.73 +/- 0.10
D0	0.60 + 0.05
D1	Ø 0.60 + 0.05
E	1.75 +/- 0.10
F	5.50 +/- 0.05
K0	0.68 +/- 0.10
P0	2.00 +/- 0.05
P1	4.00 +/- 0.10
P2	4.00 +/- 0.10
T	0.28 +/- 0.02
W	12.00 + 0.30 /- 0.10

Package Dimensions — uDFN-14 (3.5x1.35x0.5mm)

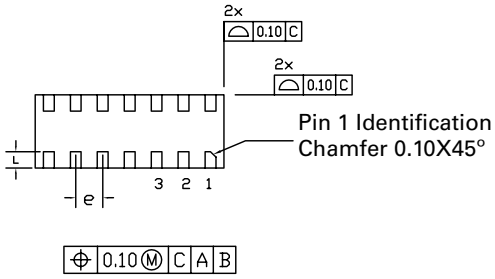
Top View



Side View



Bottom View



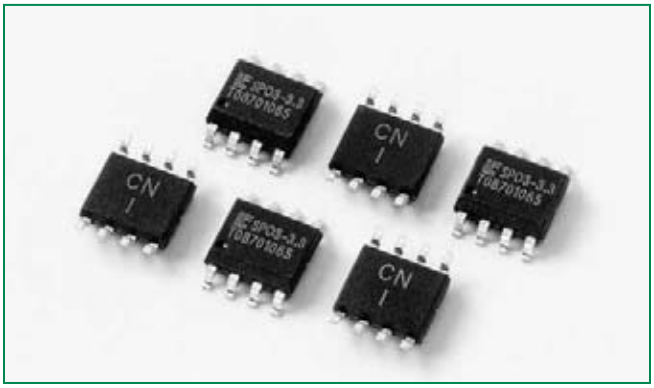
uDFN-14 (3.5x1.35x0.5mm)						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2		0.203 Ref			0.008 Ref	
b	0.15	0.20	0.25	0.006	0.008	0.012
D	3.40	3.50	3.60	0.134	0.138	0.142
D2	-	-	-	-	-	-
E	1.25	1.35	1.45	0.050	0.054	0.058
E1	-	-	-	-	-	-
e		0.500 BSC			0.020 BSC	
L	0.25	0.30	0.35	0.010	0.012	0.014

Notes:

1. Dimension and tolerancing comform to ASME Y14.5M-1994.
2. Controlling dimensions: Millimeter. Converted Inch dimensions are not necessarily exact.

SP03-3.3 Series 3.3V 150A Rail Clamp Array

HF RoHS GREEN



Description

This new broadband protection device from Littelfuse provides overvoltage protection for applications such as 10/100/1000 BaseT Ethernet, T3/E3 DS3 interfaces, ADSL2+, and VDSL2+. This new protector combines the TVS diode element with a diode rectifier bridge to provide both longitudinal and differential protection in one package. This design innovation results in a capacitive loading characteristic that is log-linear with respect to the signal voltage across the device. This reduces intermodulation (IM) distortion caused by a typical solid-state protection solution. The application schematic provides the connection information.

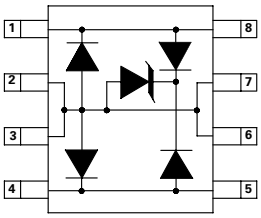
Agency Approvals - Pending

Agency	Agency File Number
®	E128662

Features

- RoHS compliant
- MS-012 surface mount package (JEDEC SO-8)
- Low insertion loss, log-linear capacitance
- Combined longitudinal and metallic protection
- Lightning Protection, IEC61000-4-5, 100A (8/20µs)
- Clamping speed of nanoseconds
- UL 94V-0 epoxy molding
- Pending UL recognized component
- Low clamping voltage

Pinout

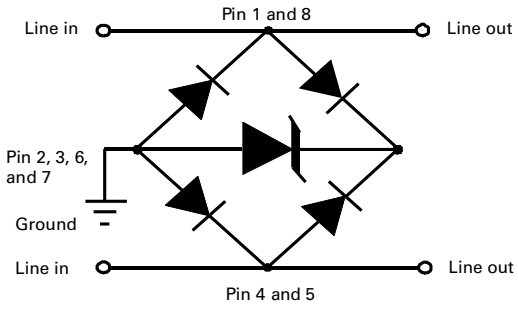


SO-8 (Top View)

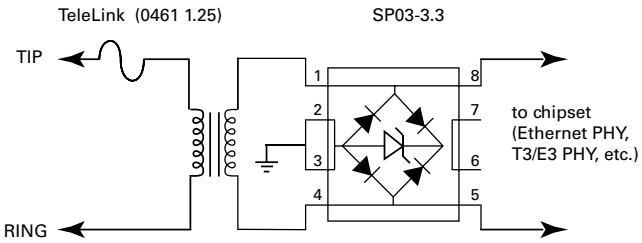
Applications

- T1/E1 Line cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet

Functional Block Diagram



Application Example



This schematic shows a high-speed data interface protection solution. The SP03-3.3 provides both metallic (differential) and longitudinal (common mode) protection from lightning induced surge events. Its surge rating is compatible with the intra-building surge requirements of Telcordia's GR-1089-CORE, and the Basic Level Recommendations of ITU K.20 and .21. This device protects against both positive and negative induced surge events. The TeleLink fuse provides overcurrent protection for the long term 50/60 Hz power fault events.

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Current (8/20µs)	150	A
Peak Pulse Power (8/20µs)	3300	W
IEC 61000-4-2, Direct Discharge, (Level 4)	30	kV
IEC 61000-4-2, Air Discharge, (Level 4)	30	kV
IEC 61000-4-5 (8/20µs)	100	A
Telcordia GR 1089 (Intra-Building) (2/10µs)	100	A
ITU K.20 (5/310µs)	40	A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
SOIC Package	170	°C/W
Operating Temperature Range	-55 to 125	°C
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s) (SOIC - Lead Tips Only)	260	°C

Electrical Characteristics (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Stand-Off Voltage	V_{RWM}	-	-	-	3.3	V
Reverse Breakdown Voltage	V_{BR}	I_T= 2µA	3.3	-	-	V
Reverse Breakdown Voltage	V_{BR}	I_T= 50µA	3.3	-	-	V
Reverse Leakage Current	I_R	V_{RWM}= 3.3V, T= 25°C	-	-	1	µA
Clamping Voltage, Line-Ground	V_C	I_{PP}= 50A, t_p=8/20 µs	-	-	11.5	V
Clamping Voltage, Line-Ground	V_C	I_{PP}= 100A, t_p=8/20 µs	-	-	15	V
Clamping Voltage, Line-Line	V_C	I_{PP}= 50A, t_p=8/20 µs	-	-	13.5	V
Clamping Voltage, Line-Line	V_C	I_{PP}= 100A, t_p=8/20 µs	-	-	18	V
Junction Capacitance	C_j	Between I/O Pins and Ground V_R=0V, f= 1MHz	-	16	25	pF
		Between I/O Pins V_R=0V, f= 1MHz	-	8	12	pF

Figure 1: Non-repetitive Peak Pulse Current vs. Pulse Time

Figure 2: Current Derating Curve

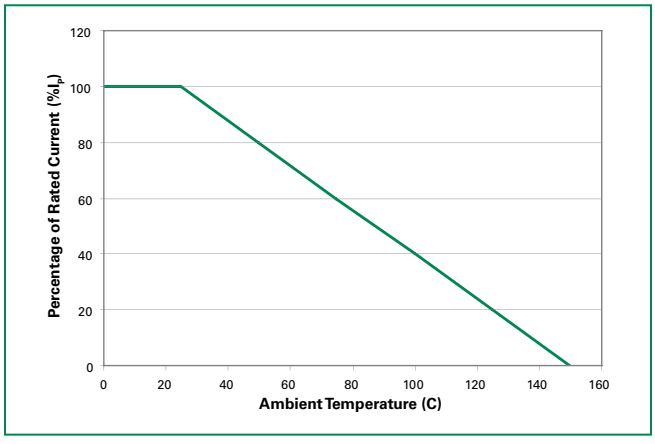


Figure 3: Pulse Waveform

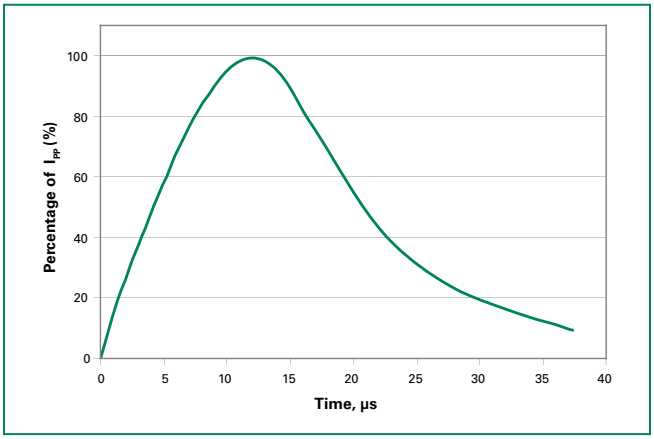


Figure 4: Clamping Voltage vs. Peak Pulse Current

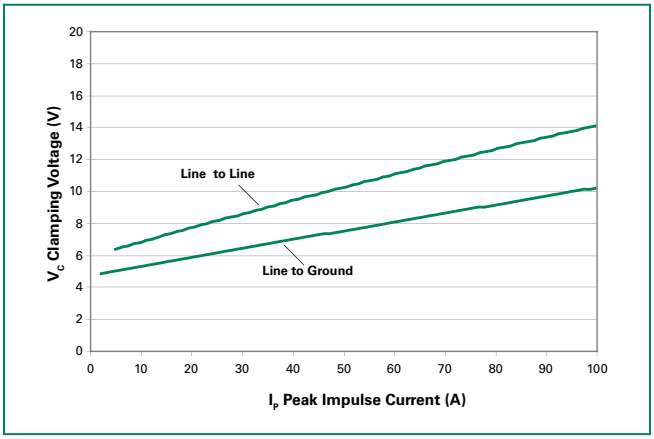


Figure 5: Capacitance vs. Reverse Voltage

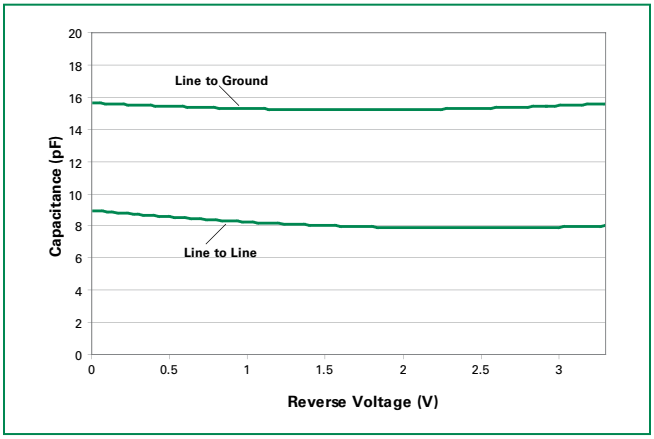
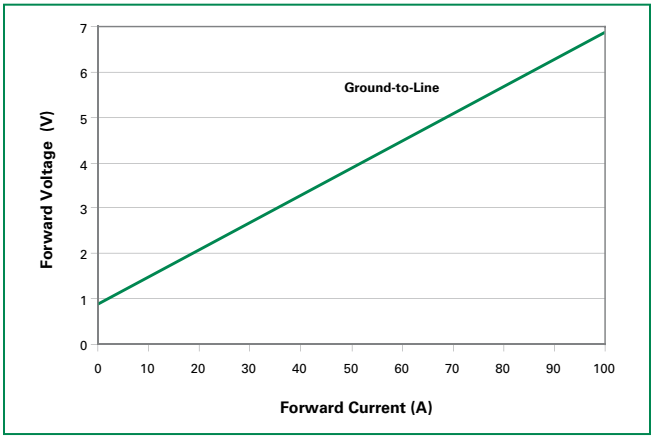
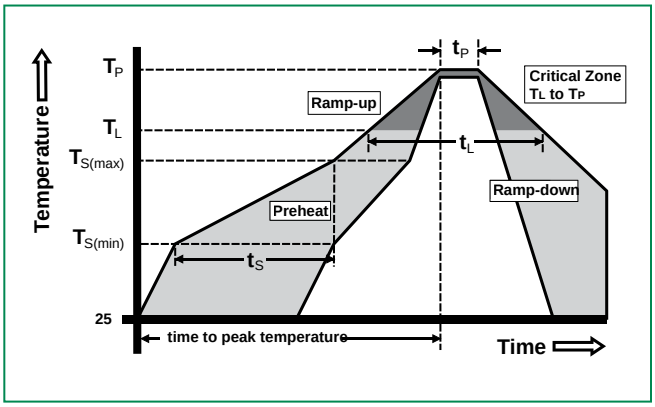


Figure 6: Forward Voltage vs. Forward Current

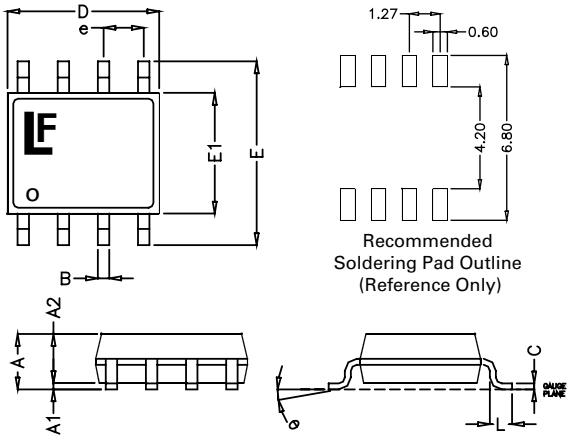


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

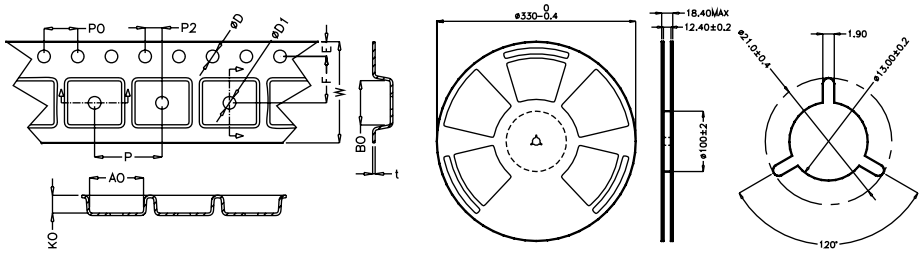


Package Dimensions — Mechanical Drawings and Recommended Solder Pad Outline



Package	MS-012 (SO-8)			
Pins	8			
JEDEC	MO-223 Issue A			
	Millimetres		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.050	0.065
B	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050

Embossed Carrier Tape & Reel Specification — SOIC Package



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

Part Numbering System

SP 03 - 3.3 B T G

- SP — Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- 03 — Series
- 3.3 — Working Voltage
- B — Package B = SOIC
- T — T= Tape & Reel
- G — G= Green

Part Marking System

First Line: Part number
Second Line: Date code

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP03-3.3BTG	SOIC Tape & Reel	SP03-3.3	2500

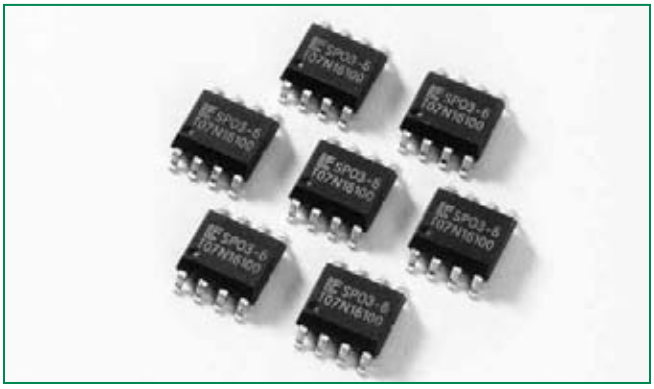
Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

SP03-6 Series 6V 150A Rail Clamp Array

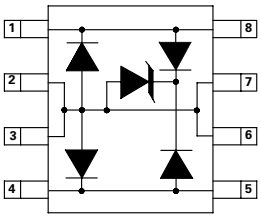
HF RoHS GREEN



Agency Approvals - Pending

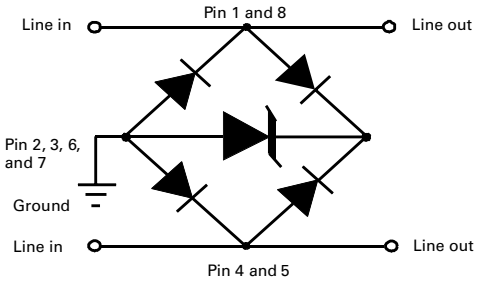
Agency	Agency File Number
®	E128662

Pinout



SO-8 (Top View)

Functional Block Diagram



Description

This new broadband protection device from Littelfuse provides overvoltage protection for applications such as 10/100/1000 BaseT Ethernet, T3/E3 DS3 interfaces, ADSL2+, and VDSL2+. This new protector combines the TVS diode element with a diode rectifier bridge to provide both longitudinal and differential protection in one package. This design innovation results in a capacitive loading characteristic that is log-linear with respect to the signal voltage across the device. This reduces intermodulation (IM) distortion caused by a typical solid-state protection solution. The application schematic provides the connection information.

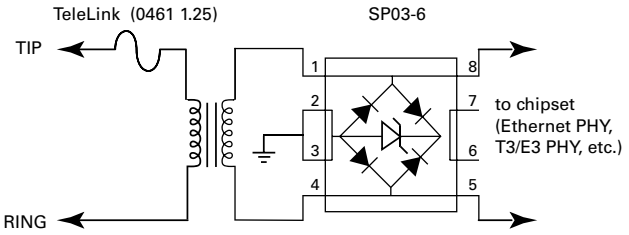
Features

- RoHS compliant
- MS-012 surface mount package (JEDEC SO-8)
- Low insertion loss, log-linear capacitance
- Combined longitudinal and metallic protection
- Clamping speed of nanoseconds
- UL 94V-0 epoxy molding
- Pending UL recognized component
- Low clamping voltage

Applications

- T1/E1 Line cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet

Application Example



This schematic shows a high-speed data interface protection solution. The SP03-6 provides both metallic (differential) and longitudinal (common mode) protection from lightning induced surge events. Its surge rating is compatible with the intra-building surge requirements of Telcordia's GR-1089-CORE, and the Basic Level Recommendations of ITU K.20 and .21. This device protects against both positive and negative induced surge events. The TeleLink fuse provides overcurrent protection for the long term 50/60 Hz power fault events.

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Current (8/20µs)	150	A
Peak Pulse Power (8/20µs)	2800	W
IEC 61000-4-2, Direct Discharge, (Level 4)	30	kV
IEC 61000-4-2, Air Discharge, (Level 4)	30	kV
IEC 61000-4-5 (8/20µs)	100	A
Telcordia GR 1089 (Intra-Building) (2/10µs)	100	A
ITU K.20 (5/310µs)	40	A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
SOIC Package	170	°C/W
Operating Temperature Range	-55 to 125	°C
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s) (SOIC - Lead Tips Only)	260	°C

Electrical Characteristics (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Stand-Off Voltage	V_{RWM}	-	-	-	6	V
Reverse Breakdown Voltage	V_{BR}	I_T= 1mA	6.8	-	-	V
Reverse Leakage Current	I_R	V_{RWM}= 6V, T= 25°C	-	-	25	µA
Clamping Voltage, Line-Ground	V_C	I_{PP}= 50A, t_p=8/20 µs	-	-	15	V
Clamping Voltage, Line-Ground	V_C	I_{PP}= 100A, t_p=8/20 µs	-	-	20	V
Junction Capacitance	C_j (Line-Ground)	Between I/O Pins and Ground V_R=0V, f= 1MHz	-	16	25	pF
	C_j (Line-Line)	Between I/O Pins V_R=0V, f= 1MHz	-	8	12	pF

Figure 1: Non-repetitive Peak Pulse Current vs. Pulse Time

Figure 2: Current Derating Curve

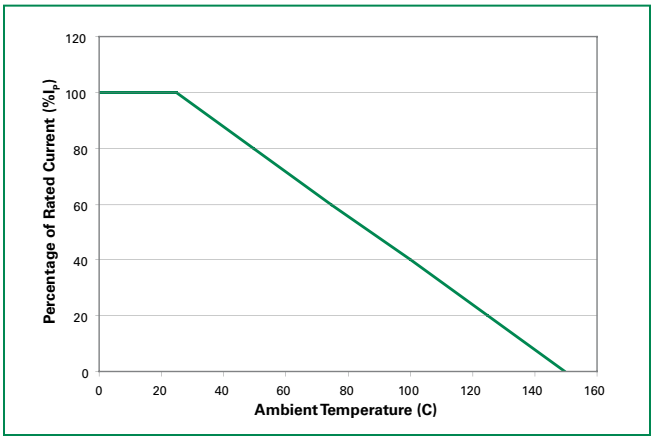


Figure 3: Pulse Waveform

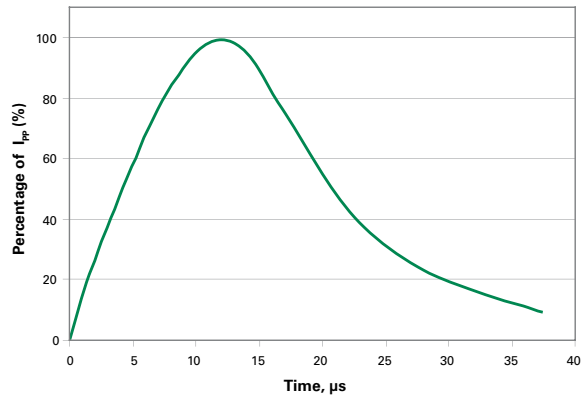


Figure 4: Clamping Voltage vs. Peak Pulse Current

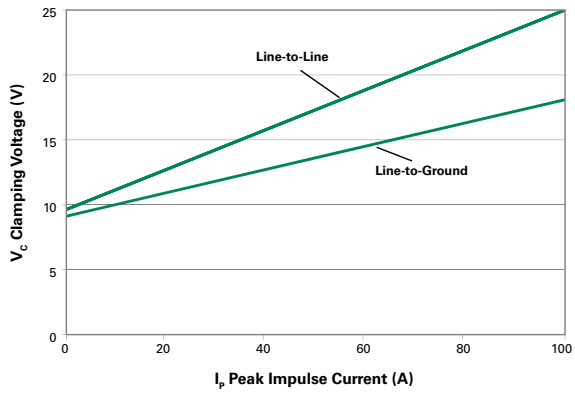


Figure 5: Capacitance vs. Reverse Voltage

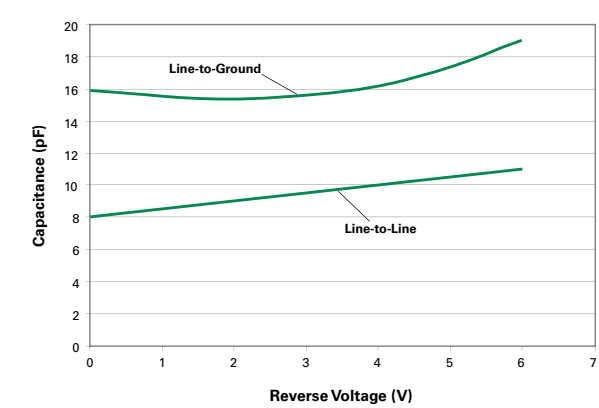
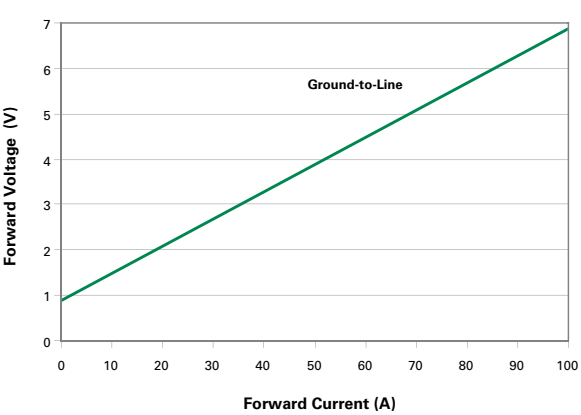
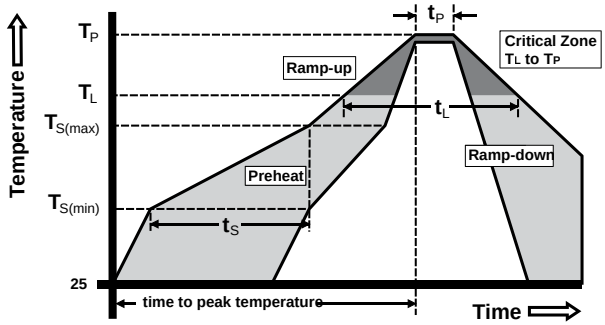


Figure 6: Forward Voltage vs. Forward Current

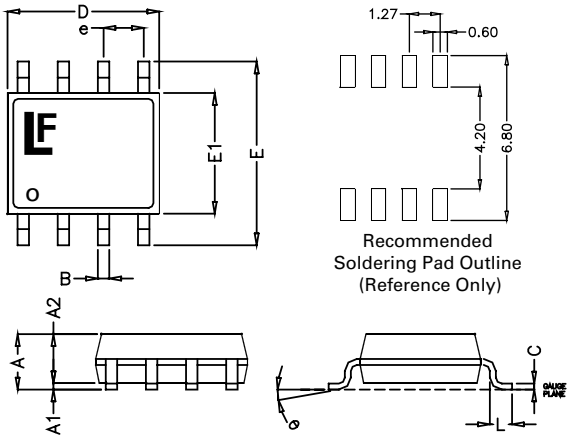


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

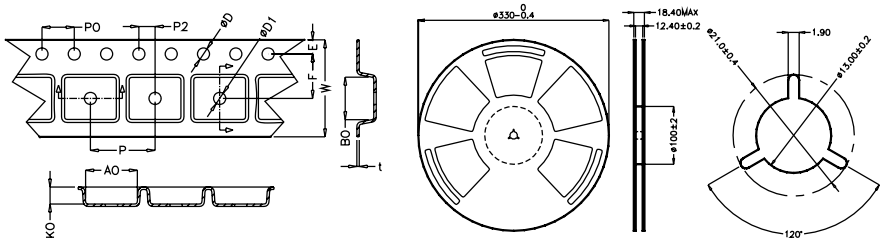


Package Dimensions — Mechanical Drawings and Recommended Solder Pad Outline



Package	MS-012 (SO-8)			
Pins	8			
JEDEC	MO-223 Issue A			
	Millimetres		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.049	0.065
B	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050

Embossed Carrier Tape & Reel Specification — SOIC Package



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

Part Numbering System

SP 03 - 6 B T G

- SP — Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- 03 — Series
- 6 — Working Voltage
- B — Package B - SOIC
- T — T= Tape & Reel
- G — G= Green

Part Marking System

First Line: Part number
Second Line: Date code

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP03-6BTG	SOIC Tape & Reel	SP03-6	2500

Product Characteristics

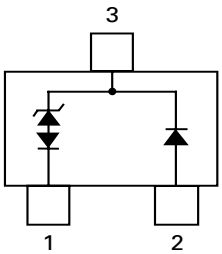
Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

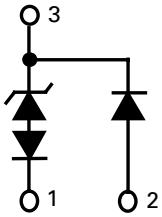
SPLV2.8 Series 2.8V 40A TVS Array

HF RoHS GREEN

Pinout



Functional Block Diagram



Description

The SPLV2.8 was designed to protect low voltage, CMOS devices from ESD and lightning induced transients. There is a compensating diode in parallel with the low voltage TVS to protect one unidirectional line or a high speed data pair when two devices are paired together. These robust structures can safely absorb repetitive ESD strikes at ±30kV (contact discharge) per the IEC61000-4-2 standard and each structure can safely dissipate up to 40A (IEC61000-4-5, t_p=8/20µs) with very low clamping voltages.

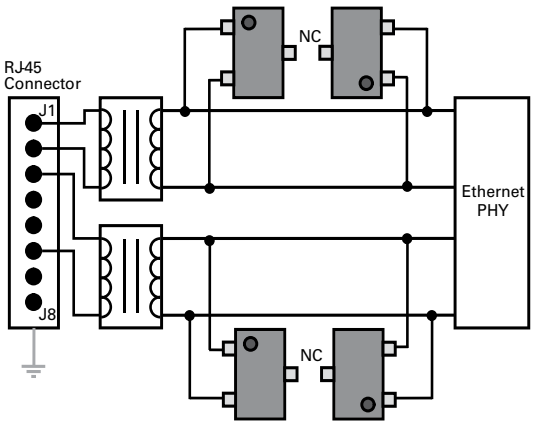
Features

- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 40A (8/20µs)
- Low capacitance of 2pF per line (Pin 2 to 1)
- Low leakage current of 1µA (MAX) at 2.8V
- Small SOT23-3 package saves board space

Applications

- 10/100/1000 Ethernet
- WAN/LAN Equipment
- Switching Systems
- Desktops, Servers, and Notebooks
- Analog Inputs
- Base Stations

Application Example



See Application Example Detail section on page 135 for more information

Electrical Characteristics (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	I_R≤1µA			2.8	V
Reverse Breakdown Voltage	V_{BR}	I_T=2µA	3.0			V
Snap Back Voltage	V_{SB}	I_T=50mA	2.8			V
Reverse Leakage Current	I_{LEAK}	V_R=2.8V (Pin 2 or 3 to 1)			1	µA
Clamping Voltage[1]	V_C	I_{PP}=5A, t_P=8/20µs (Pin 3 to 1)		5.7	7.0	V
Clamping Voltage[1]		I_{PP}=24A, t_P=8/20µs (Pin 3 to 1)		8.3	12.5	V
Clamping Voltage[1]		I_{PP}=5A, t_P=8/20µs (Pin 2 to 1)		7.0	8.5	V
Clamping Voltage[1]		I_{PP}=24A, t_P=8/20µs (Pin 2 to 1)		13.9	15.0	V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$ (Pin 2 to 1)		0.4		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±30			kV
		IEC61000-4-2 (Air)	±30			kV
Diode Capacitance[1]	C_D	V_R=0V, f=1MHz (Pin 2 to 1)		2.0	2.5	pF

Note: [1]Parameter is guaranteed by design and/or device characterization.

Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Power (t_P=8/20µs)	600	W
Peak Pulse Current (t_P=8/20µs)	40	A
Operating Temperature	-40 to 85	°C
Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Figure 1: Capacitance vs. Reverse Voltage

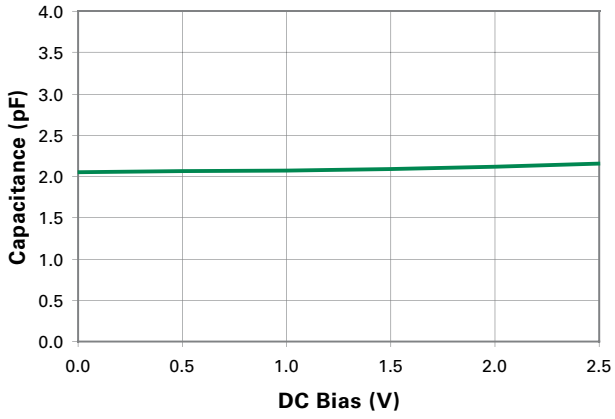


Figure 2: Clamping Voltage vs. I_{PP}

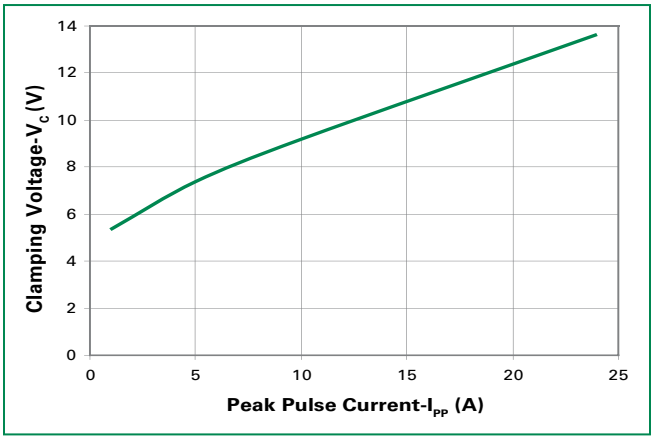
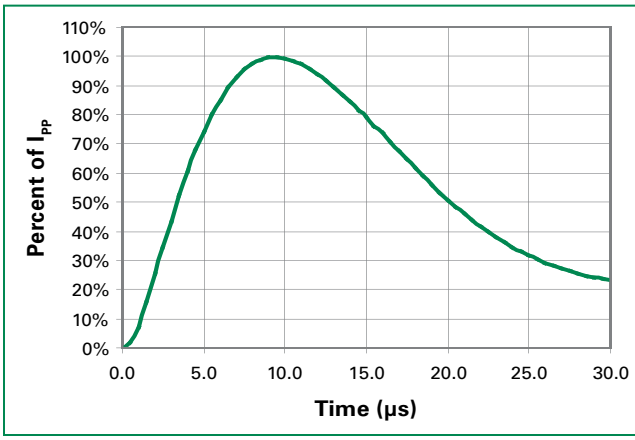
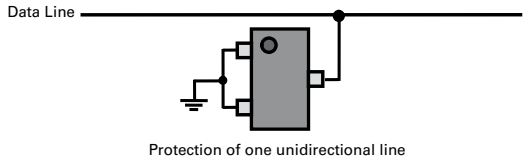


Figure 3: Pulse Waveform

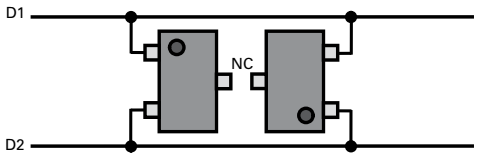


Application Example Detail



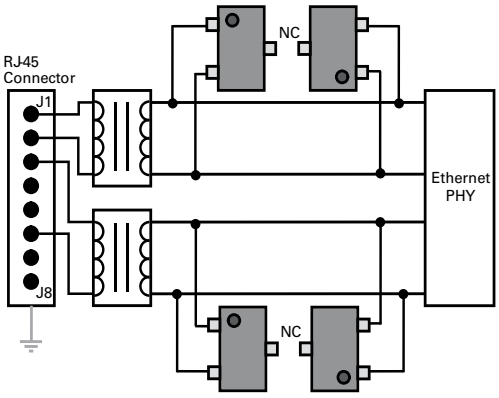
Protection of one unidirectional line

Protection of one unidirectional data line is realized by connecting pin 3 to the protected line, and pins 1 and 2 to GND. In this configuration, the device presents a maximum loading capacitance of tens of picofarads. During positive transients, the internal TVS diode will conduct and steer current from pin 3 to 1 (GND), clamping the data line at or below the specified voltages for the device (see Electrical Characteristics section). For negative transients, the internal compensating diode is forward biased, steering the current from pin 2 (GND) to 3.



Low capacitance protection of one high speed data pair

Low capacitance protection of a high-speed data pair is realized by connecting two devices in antiparallel. As shown, pin 1 of the first device is connected to D1 and pin 2 is connected to D2. Additionally, pin 2 of the second device is connected to D1 and pin 1 is connected to D2. Pin 3 must be NC (or not connected) for both devices. When the potential on D1 exceeds the potential on D2 (by the rated standoff voltage), pin 2 on the second device will steer current into pin 1. The compensating diode will conduct in the forward direction steering current into the avalanching TVS diode which is operating in the reverse direction. For the opposite transient, the first device will behave in the same manner. In this two device arrangement, the total loading capacitance is two times the rated capacitance from pin 2 to pin 1 which will typically be much less than 10pF making it suitable for high-speed data pair such as 10/100/1000 Ethernet.



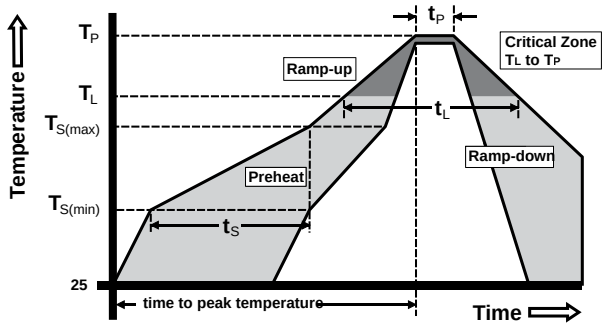
Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

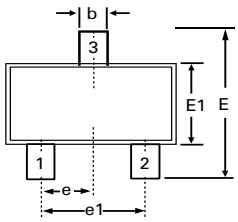
Soldering Parameters

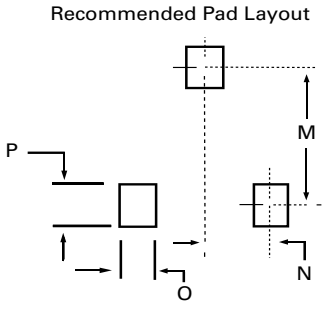
Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



SPLV2.8

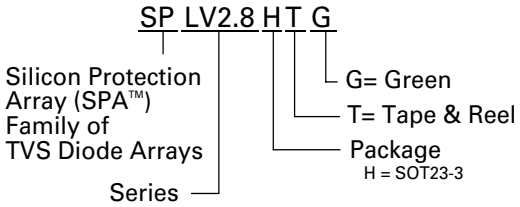
Package Dimensions — SOT-23



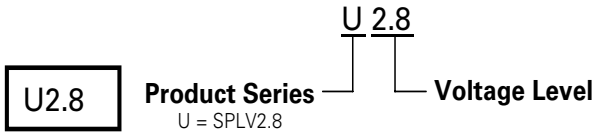


Package	SOT23-3			
Pins	3			
JEDEC	TO-236			
	Millimetres		Inches	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A1	0.01	0.1	0.0004	0.004
b	0.3	0.5	0.012	0.020
c	0.08	0.2	0.003	0.008
D	2.8	3.04	0.110	0.120
E	2.1	2.64	0.083	0.104
E1	1.2	1.4	0.047	0.055
e	0.95 BSC		0.038 BSC	
e1	1.90 BSC		0.075 BSC	
L1	0.54 REF		0.021 REF	
M		2.29		.90
N		0.95		0.038
O		0.78		0.30 TYP
P		0.78		0.30 TYP

Part Numbering System



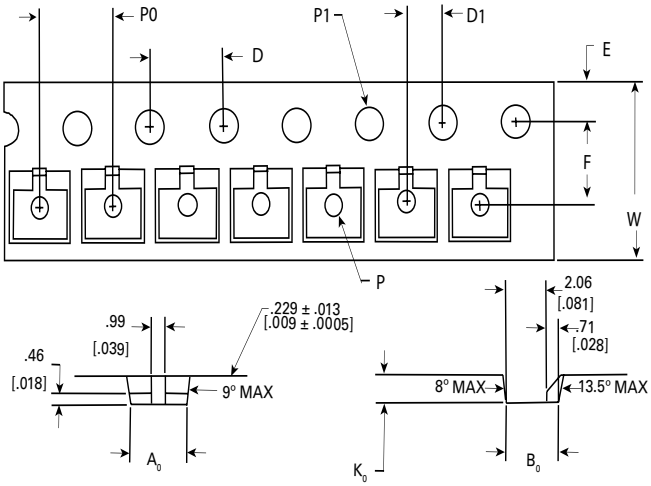
Part Marking System



Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SPLV2.8HTG	SOT23-3	U2.8	3000

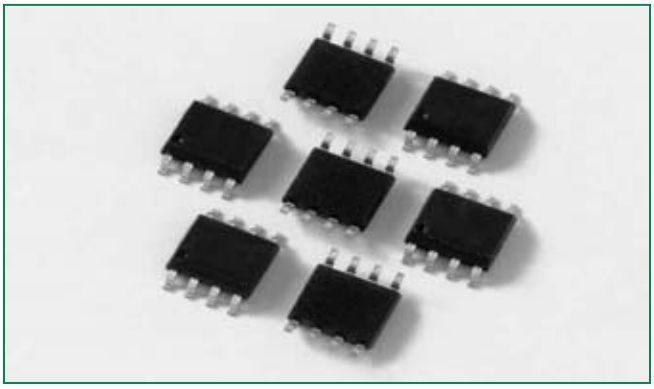
Embossed Carrier Tape & Reel Specification — SOT23-3 Package



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
A0	3.05	3.25	0.12	0.128
B0	2.67	2.87	0.105	0.113
D	3.9	4.1	0.153	0.161
D1	1.95	2.05	0.788	0.792
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.136	0.14
K0	1.12	1.32	0.476	0.484
P	0.95	1.05	0.037	0.041
P0	3.9	4.1	0.153	0.161
P1		1.6		0.063
W	7.9	8.3	0.311	0.327

SPLV2.8-4 Series 2.8V 40A TVS Array

HF RoHS GREEN



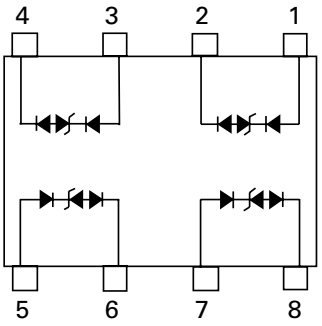
Description

The SPLV2.8-4 was designed to protect low voltage, CMOS devices from ESD and lightning induced transients. There is a compensating diode in series with each low voltage TVS to present a low loading capacitance to the line being protected. These robust structures can safely absorb repetitive ESD strikes at ±30kV (contact discharge) per IEC61000-4-2 standard and each structure can safely dissipate up to 40A (IEC61000-4-5, t_P=8/20μs) with very low clamping voltages.

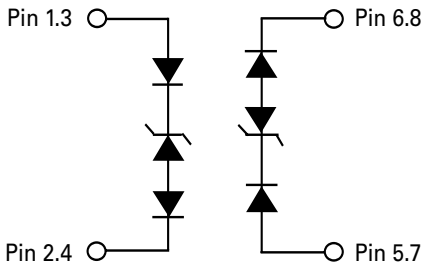
Features

- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 40A (8/20μs)
- Low capacitance of 2pF per line
- Low leakage current of 1μA (MAX) at 2.8V
- SOIC-8 pin configuration allows for simple flow-through layout

Pinout



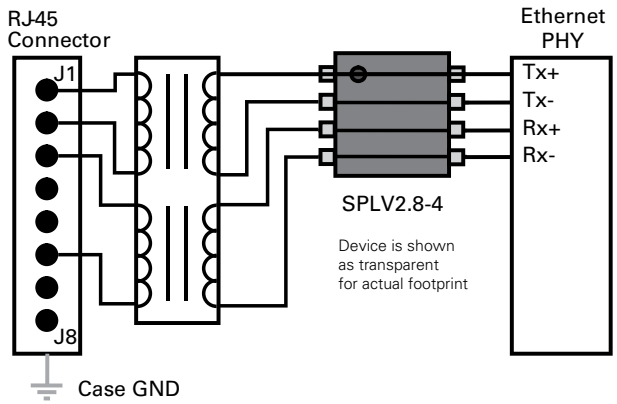
Functional Block Diagram



Applications

- 10/100/1000 Ethernet
- WAN/LAN Equipment
- Switching Systems
- Desktops, Servers, and Notebooks
- Analog Inputs
- Base Stations

Application Example



Electrical Characteristics (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	I_R≤1µA			2.8	V
Reverse Breakdown Voltage	V_{BR}	I_T=2µA	3.0			V
Snap Back Voltage	V_{SB}	I_T=50mA	2.8			V
Reverse Leakage Current	I_{LEAK}	V_R=2.8V (Each Line)			1	µA
Clamping Voltage[1]	V_C	I_{PP}=5A, t_P=8/20µs (Each Line)		7.0	8.5	V
Clamping Voltage[1]	V_C	I_{PP}=24A, t_P=8/20µs (Each Line)		13.9	15.0	V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±30			kV
		IEC61000-4-2 (Air)	±30			kV
Dynamic Resistance	R_{DYN}	(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1}) (Each Line)		0.4		Ω
Diode Capacitance[1]	C_D	V_R=0V, f=1MHz (Each Line)		2.0	2.5	pF

Note: [1]Parameter is guaranteed by design and/or device characterization.

Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Power (t_P=8/20µs)	600	W
Peak Pulse Current (t_P=8/20µs)	40	A
Operating Temperature	-40 to 85	°C
Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Figure 1: Capacitance vs. Reverse Voltage

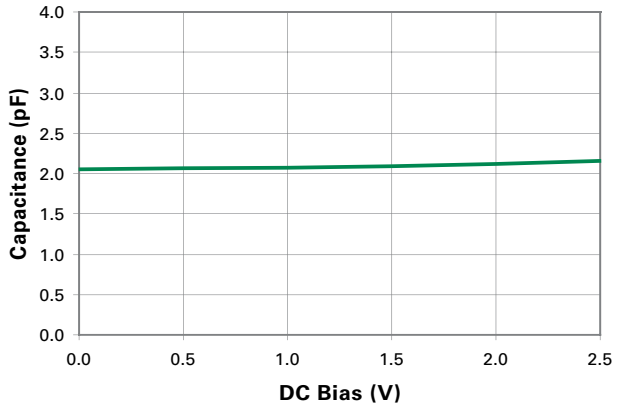


Figure 2: Clamping Voltage vs. I_{PP}

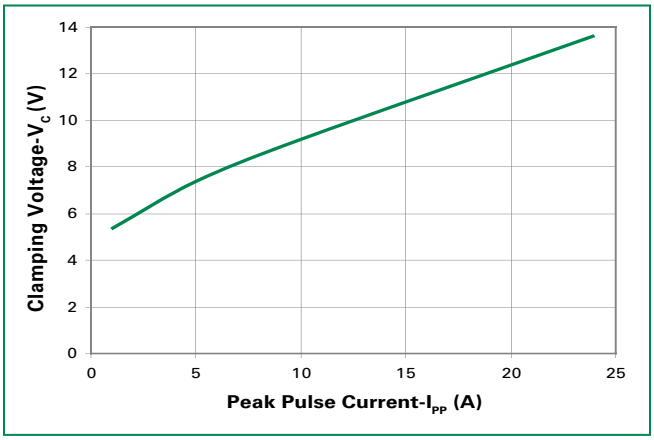
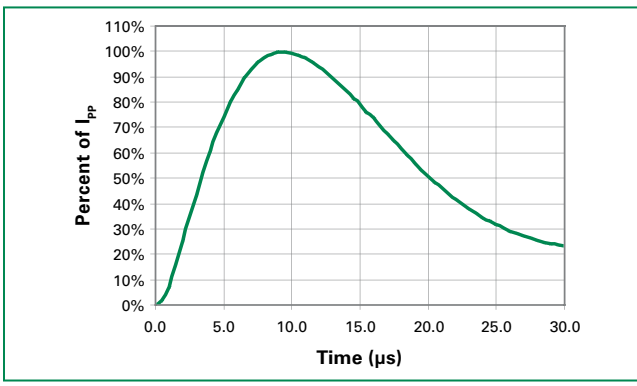


Figure 3: Pulse Waveform



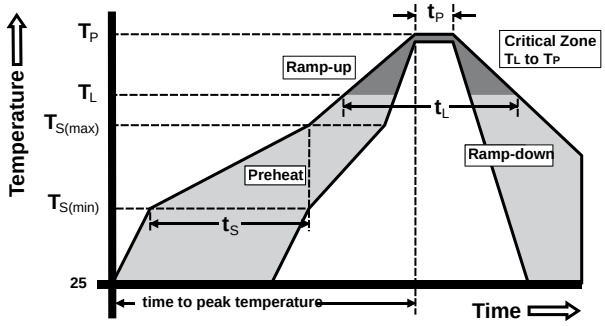
Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

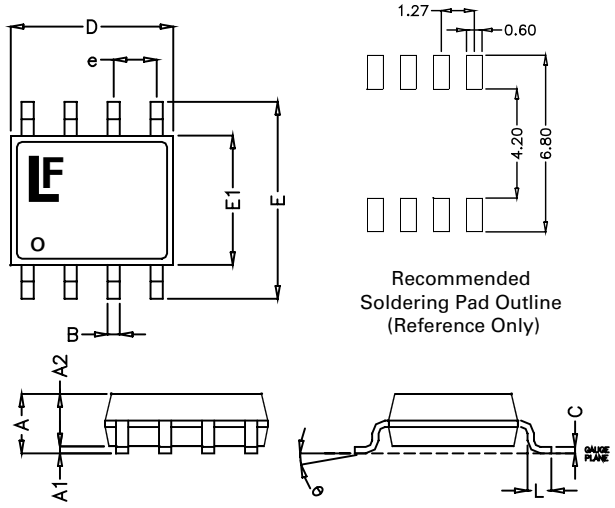
Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

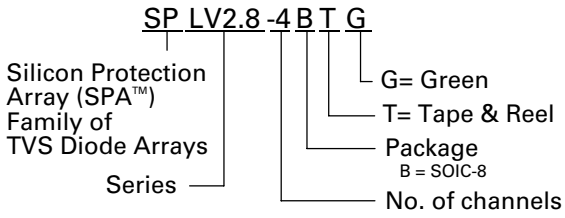


Package Dimensions — Mechanical Drawings and Recommended Solder Pad Outline

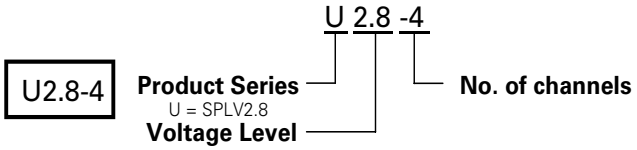


Package	MS-012 (SO-8)			
Pins	8			
JEDEC	MO-223 Issue A			
	Millimetres		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.050	0.065
B	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050

Part Numbering System



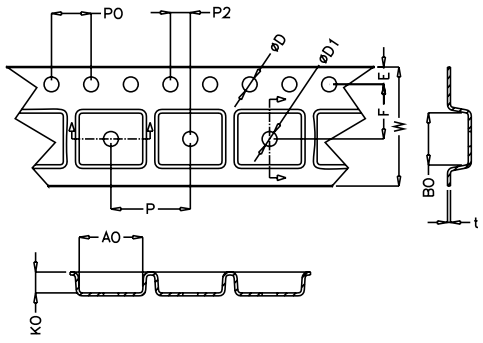
Part Marking System

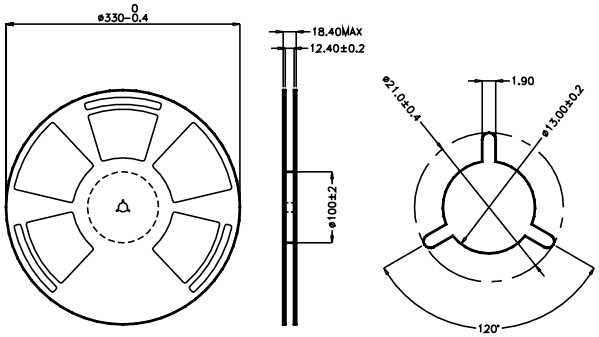


Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SPLV2.8-4BTG	SOIC-8	U2.8-4	2500

Embossed Carrier Tape & Reel Specification — SOIC Package

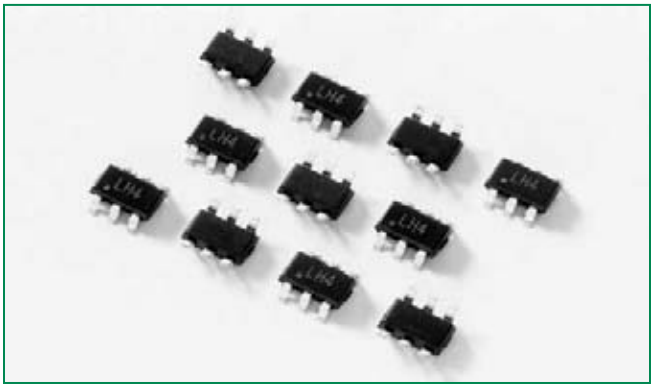




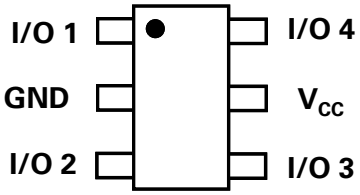
Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

SP3050 Series 6V 10A Rail Clamp Array

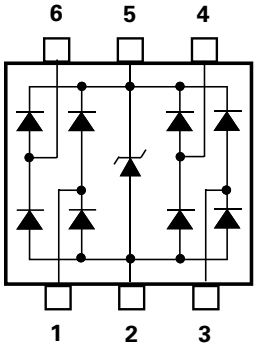
HF RoHS GREEN



Pinout



Functional Block Diagram



Description

The SP3050 integrates low capacitance rail-to-rail diodes with an additional zener diode to protect each I/O pin against ESD and high surge events. This robust device can safely absorb surge current per IEC61000-4-5 (t_p=8/20µs) without performance degradation and a minimum ±20kV ESD per IEC61000-4-2. Their very low loading capacitance also makes them ideal for protecting high speed signal pins.

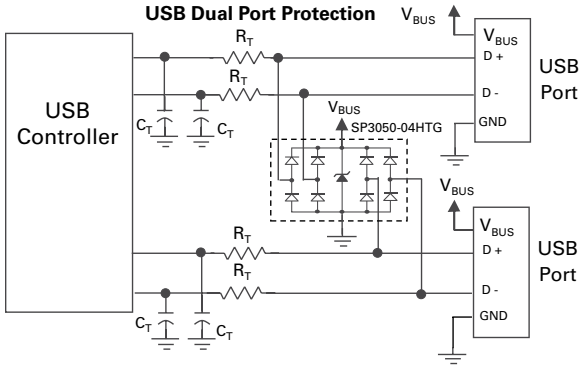
Features

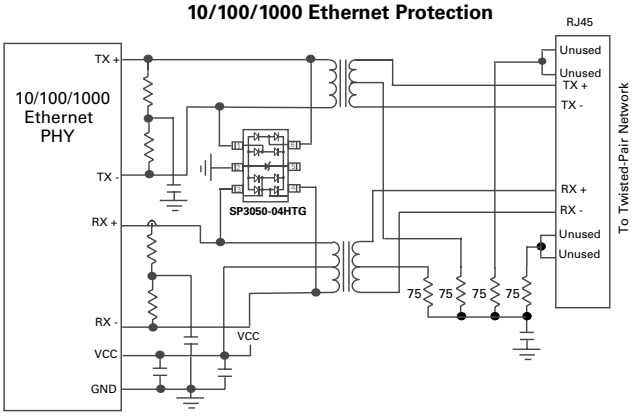
- ESD, IEC61000-4-2, ±20kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 10A (8/20µs)
- Low capacitance of 2pF (TYP) per I/O
- Low leakage current of 0.5µA (MAX) at 5V
- Small SOT23-6 packaging

Applications

- LCD/PDP TVs
- Monitors
- Notebooks
- 10/100/1000 Ethernet
- Firewire
- Set Top Boxes
- Flat Panel Displays
- Portable Medical

Application Examples





Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)[1]	10	A
P_{PK}	Peak Pulse Power (t_p=8/20µs)	150	W
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

[1]Non-repetitive pulse per waveform on page 3

Thermal Information

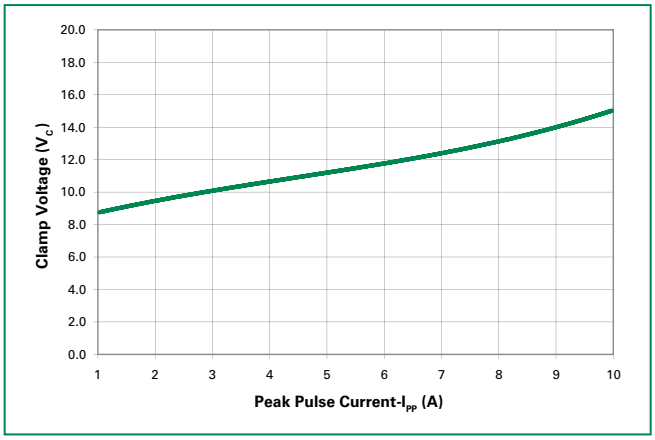
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	$I_R \leq 1\mu A$			6.0	V
Reverse Voltage Drop	V_R	I_R = 1mA		8.0		V
Reverse Leakage Current	I_{LEAK}	V_R=5V		0.1	0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, I/O to GND[2]		8.8	10.0	V
		I_{PP}=5A, t_p=8/20µs, I/O to GND[2]		11.5	13.0	V
		I_{PP}=8A, t_p=8/20µs, I/O to GND[2]		13.2	15.0	V
Dynamic Resistance	R_{DYN}	$(V_{C2} - V_{C1}) / (I_{PP2} - I_{PP1})$		0.7		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±20			kV
		IEC61000-4-2 (Air)	±30			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V		2.4	3.0	pF
		Reverse Bias=1.65V		2.0		pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		1.2		pF

Notes: [1] Parameter is guaranteed by design and/or device characterization.
[2] Repetitive pulse per waveform on page 3.

Clamping Voltage vs. I_{PP}

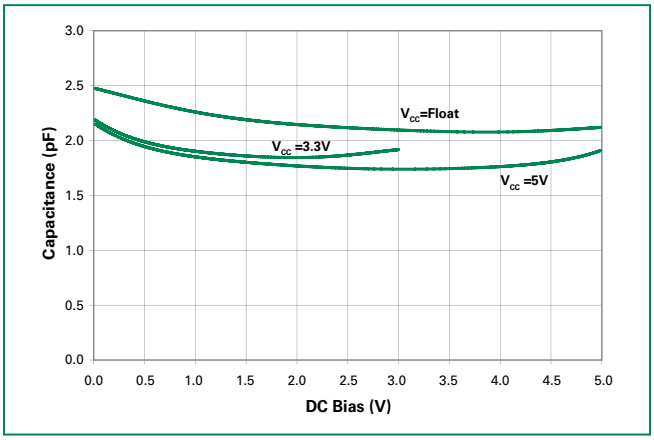


Product Characteristics

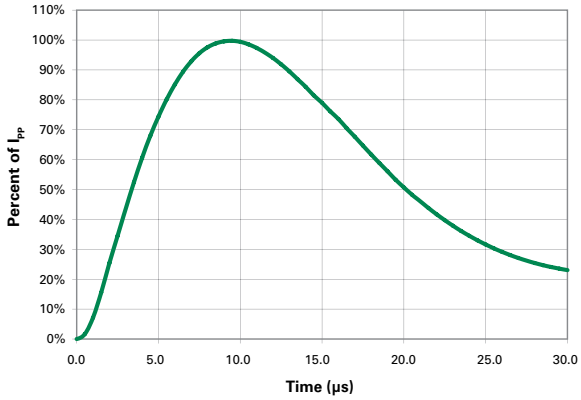
Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Capacitance vs. Reverse Bias

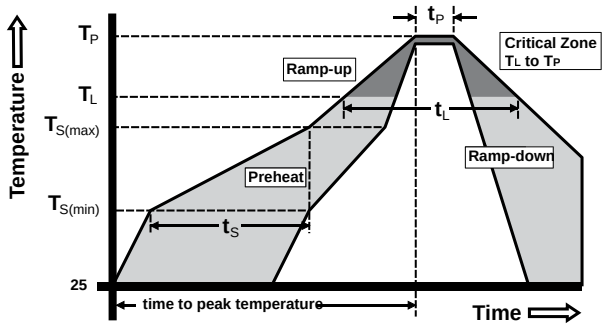


Pulse Waveform



Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

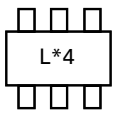


Part Numbering System

SP 3050 - 04 H T G

- SP 3050: Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- 04: Number of Channels
- H: Package H: SOT23-6
- T: T= Tape & Reel
- G: G= Green

Part Marking System



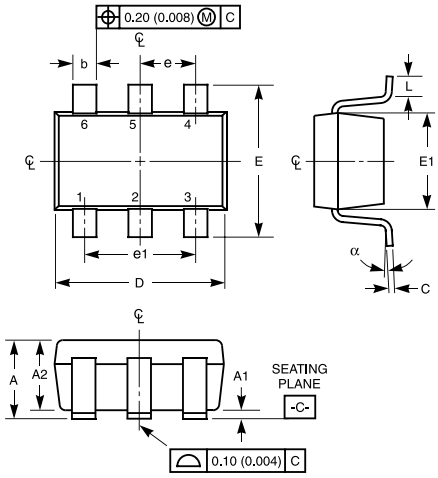
L * 4

- L: Product Series L = SP3050
- *: Assembly Site (Varies)
- 4: Number of Channels

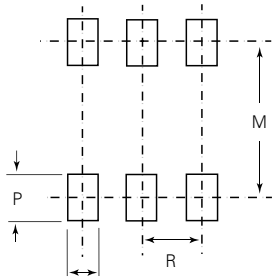
Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3050-04HTG	SOT23-6	L*4	3000

Package Dimensions — SOT23-6



Recommended Solder Pad Layout

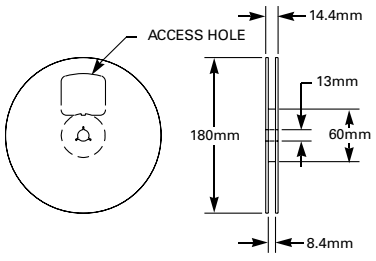


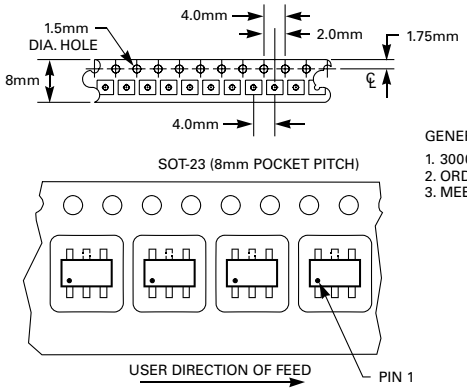
Package	SOT23-6				
Pins	6				
JEDEC	MO-203 Issue A				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	0.900	1.450	0.035	0.057	-
A1	0.000	0.150	0.000	0.006	-
A2	0.900	1.300	0.035	0.051	-
b	0.350	0.500	0.0138	0.0196	-
C	0.080	0.220	0.0031	0.009	-
D	2.800	3.000	0.11	0.118	3
E	2.600	3.000	0.102	0.118	-
E1	1.500	1.750	0.06	0.069	3
e	0.95 Ref		0.0374 ref		-
e1	1.9 Ref		0.0748 Ref		-
L	0.100	0.600	0.004	0.023	4,5
N	6		6		6
a	0°	10°	0°	10°	-
M		2.590		0.102	-
O		0.690		.027 TYP	-
P		0.990		.039 TYP	-
R		0.950		0.038	-

Notes:
1. Dimensioning and tolerances per ANSI 14.5M-1982.
2. Package conforms to EIAJ SC-74 (1992).
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlenth L measured at reference to seating plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Embossed Carrier Tape & Reel Specification — SOT23-6

8mm TAPE AND REEL



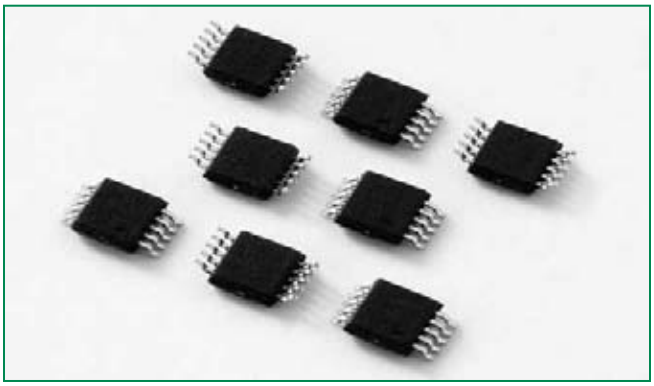


GENERAL INFORMATION

1. 3000 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

SP4060 Series 2.5V 20A Rail Clamp Array

HF RoHS GREEN



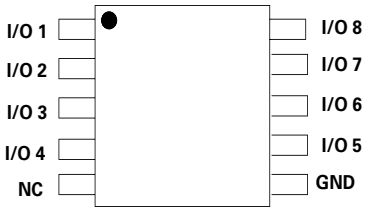
Description

The SP4060 integrates low capacitance diodes with an additional zener diode to protect each I/O pin against ESD and high surge events. This robust device can safely absorb up to 20A per IEC61000-4-5 (t_p=8/20µs) without performance degradation and a minimum ±30kV ESD per IEC61000-4-2 International Standard. Their low loading capacitance also makes them ideal for protecting high speed signal pins.

Features

- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC61000-4-4, 40A (5/50ns)
- Lightning, IEC61000-4-5, 20A (8/20µs)
- Low capacitance of 4.4pF (TYP) per I/O
- Low leakage current of 1µA (MAX) at 2.5V

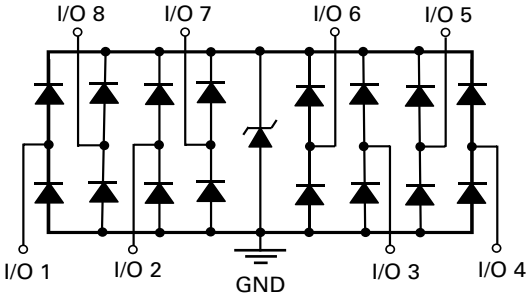
Pinout



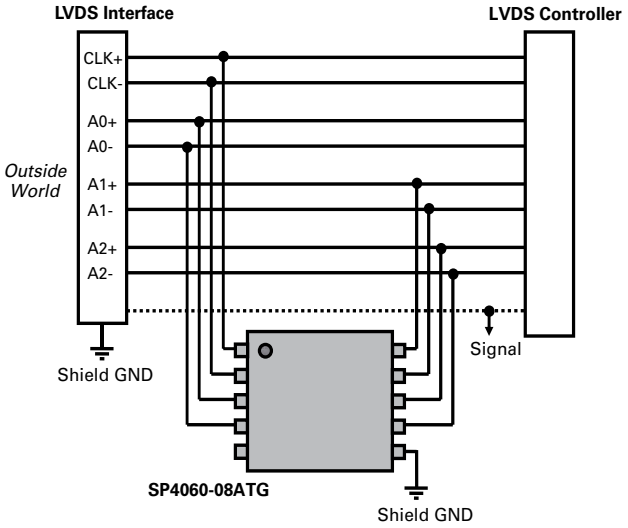
Applications

- LCD/PD TVs
- Desktops
- Game Consoles
- Set Top Boxes
- Notebooks

Functional Block Diagram



Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current (t_p=8/20µs)	20.0	A
P_{PK}	Peak Pulse Power (t_p=8/20µs)	300	W
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

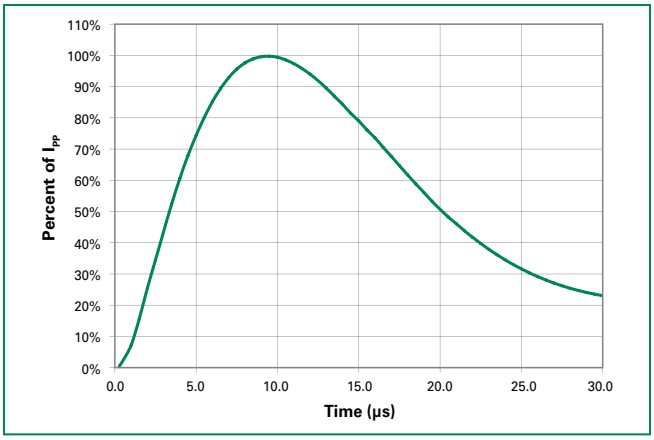
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

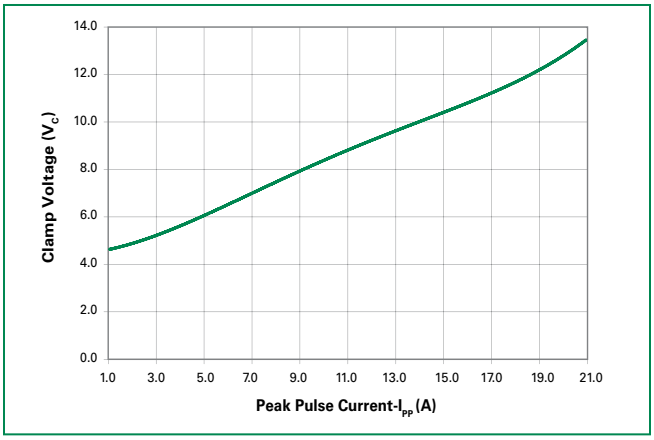
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}				2.5	V
Snap Back Voltage	V_{SB}	I_{SB}=50mA	2.0			V
Reverse Leakage Current	I_{LEAK}	V_R=2.5V, I/O to GND		0.5	1.0	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		4.5	5.5	V
		I_{PP}=5A, t_p=8/20µs, Fwd		6.0	7.2	V
		I_{PP}=10A, t_p=8/20µs, Fwd		8.0	9.6	V
		I_{PP}=20A, t_p=8/20µs, Fwd		12.5	15.0	V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±30			kV
		IEC61000-4-2 (Air)	±30			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V		4.4	5.0	pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		2.2		pF

Note: [1] Parameter is guaranteed by design and/or device characterization.

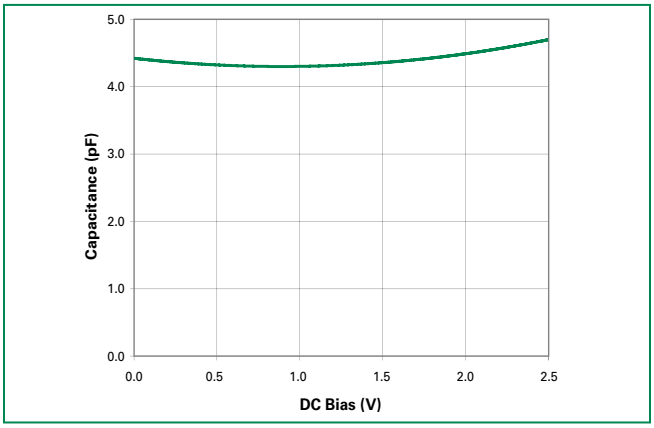
Pulse Waveform



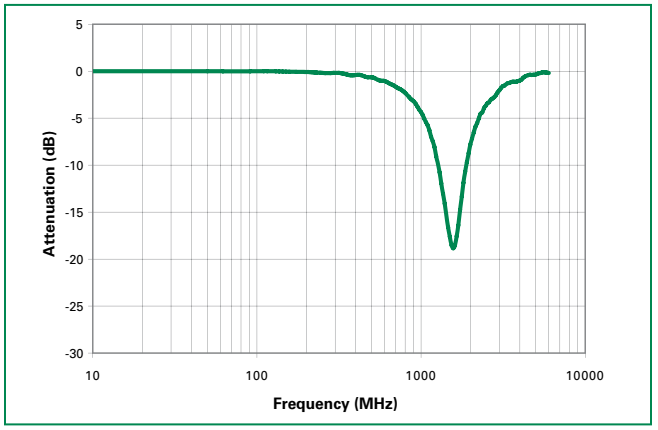
Clamping Voltage vs. I_{PP}



Capacitance vs. Bias

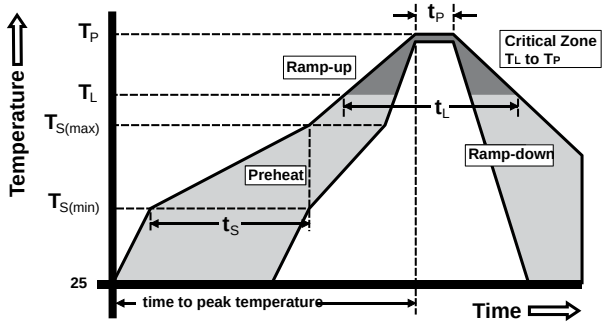


Insertion Loss (S21) I/O to GND

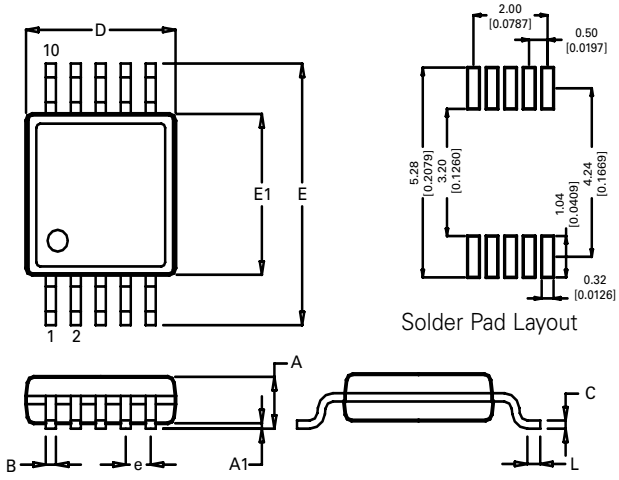


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

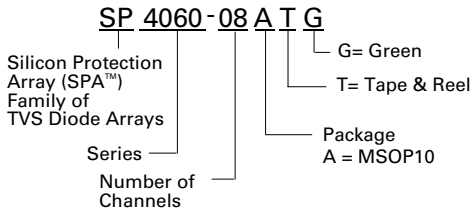


Package Dimensions — MSOP10

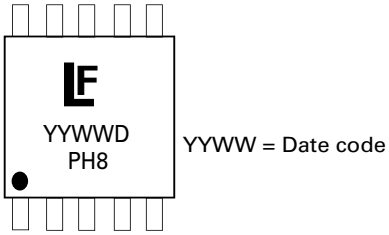


Package	MSOP10			
Pins	10			
	Millimeters		Inches	
DIM	Min	Max	Min	Max
A	-	1.10	-	0.043
A1	0.00	0.15	0.000	0.006
B	0.17	0.27	0.007	0.011
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.67	5.10	0.184	0.200
E1	2.90	3.10	0.114	0.122
e	0.50 BSC		0.020 BSC	
L	0.40	0.80	0.016	0.032

Part Numbering System



Part Marking System



Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

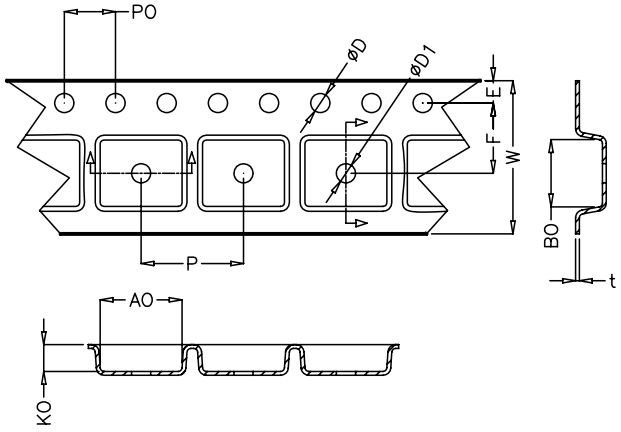
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP4060-08ATG	MSOP10	PH8	4000

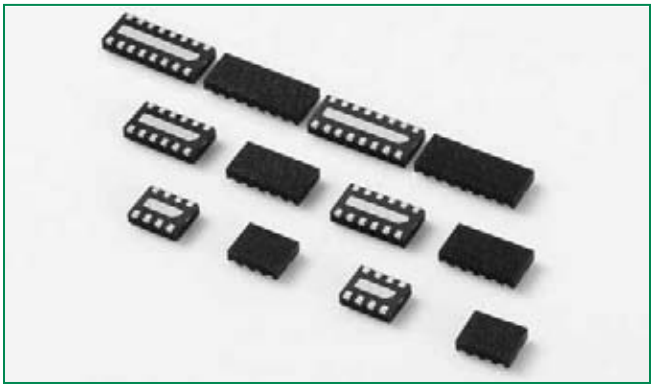
Embossed Carrier Tape & Reel Specification — MSOP-10



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.40	5.60	0.213	0.220
D	1.50	1.60	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.90	4.10	0.154	0.161
10P0	40.0+/- 0.20		1.574+/-0.008	
W	11.90	12.10	0.469	0.476
P	7.90	8.10	0.311	0.319
A0	5.20	5.40	0.205	0.213
B0	3.20	3.40	0.126	0.134
K0	1.20	1.40	0.047	0.055
t	0.30 +/- 0.05		0.012+/- 0.002	

SP6001 Series 12pF 30kV EMI Filter Array

HF RoHS GREEN



Description

The Littelfuse SP6001 SPA series integrates 4, 6 and 8 EMI filters (C-R-C) into a small, low-profile UDFN package with each filter providing greater than -30dB attenuation at 1GHz. Additionally, each I/O is capable of shunting ±30kV ESD strikes (IEC61000-4-2, contact discharge) away from sensitive electronic components. The performance of this small, slim design makes it extremely suitable for mobile handsets, PDAs and notebook computers.

Features

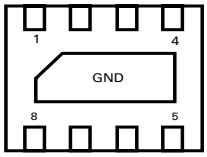
- EMI filtering of frequencies from 800MHz to 3GHz
- Greater than -30dB attenuation (TYP) at 1GHz
- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- Small, low-profile UDFN package (TYP 0.5mm height)

Applications

- Keypad interface for portable electronics
- LCD and camera display interfaces for handsets
- Connector interfaces for portable electronics
- Mobile phone
- Smartphone
- Portable navigation device

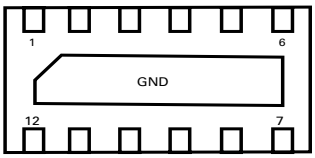
Pinout

UDFN-08



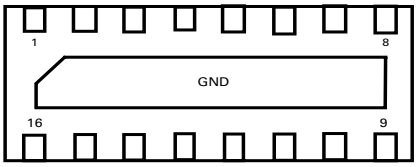
SP6001-04UTG-1

UDFN-12



SP6001-06UTG-1

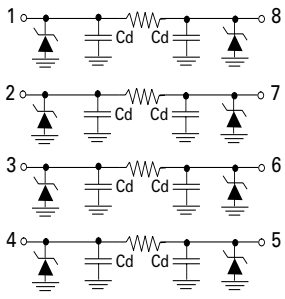
UDFN-16



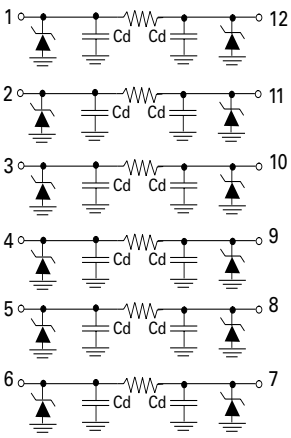
SP6001-08UTG-1

Functional Block Diagram

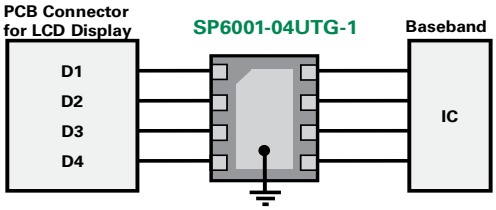
SP6001-04UTG-1

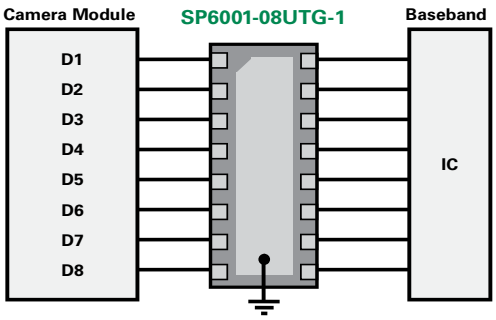


SP6001-06UTG-1



Application Examples





Absolute Maximum Ratings

Symbol	Parameter	Value	Units
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

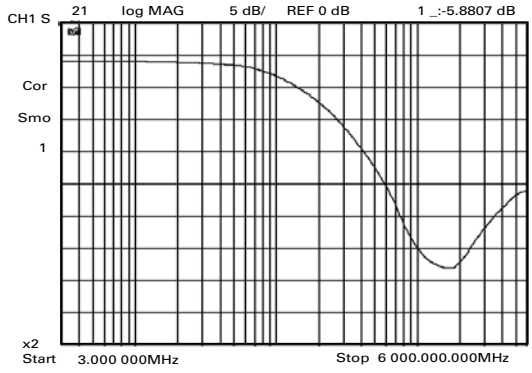
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

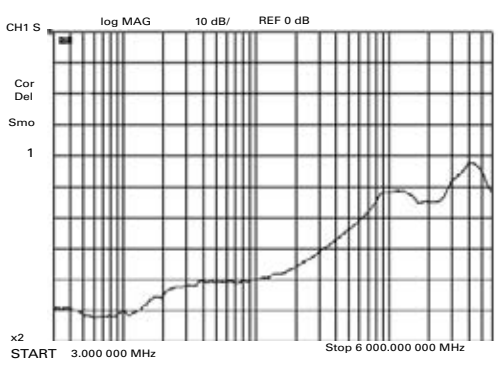
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}				6.0	V
Breakdown Voltage	V_{BR}	I_R=1mA	7.0 (90%TYP)	7.8	8.5 (109%TYP)	V
Reverse Leakage Current	I_{LEAK}	V_{RWM}=5V		0.1	1.0	µA
Resistance	R_A	I_R=10mA	85 (85%TYP)	100	115 (115% TYP)	Ω
Diode Capacitance[1,2]	C_D	V_R=2.5V,f=1MHz		12		pF
Line Capacitance[1,2]	C_L	V_R=2.5V,f=1MHz	19 (79.2%TYP)	24	29 (120.8%TYP)	pF
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact Discharge)	±30			kV
		IEC61000-4-2 (Air Discharge)	±30			kV
Cutoff Frequency[3]	F_{-3dB}	Above this frequency, appreciable attenutation occurs		115		MHz

Notes: [1] Parameter is guaranteed by design and/or device characterization.
[2] Total line capacitance is two times the diode capacitance (C_D).
[3] 50Ω source and 50Ω load termination

Insertion Loss (S21)



Analog Crosstalk (S41)

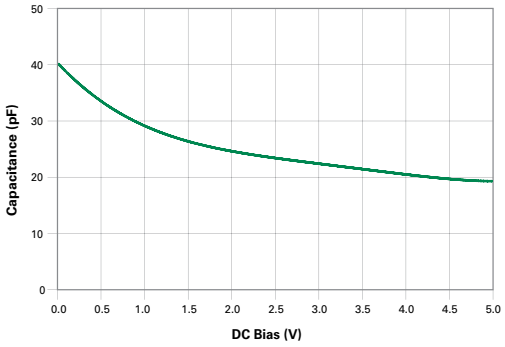


Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

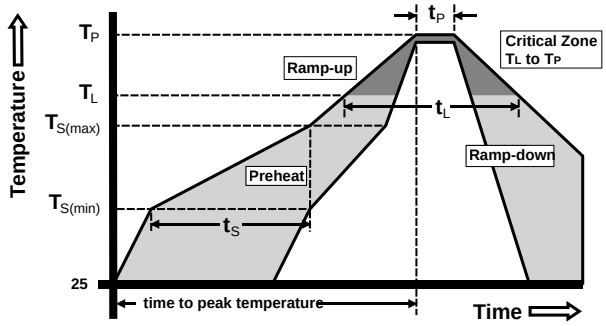
Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Line Capacitance vs. DC Bias

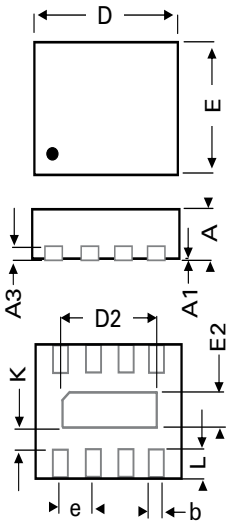


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

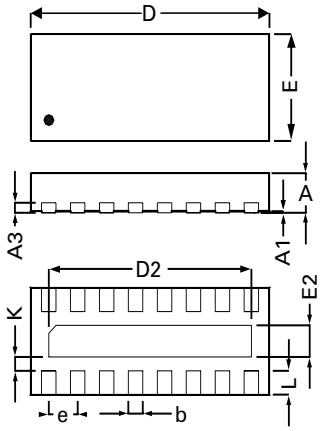


Package Dimensions — UDFN-08



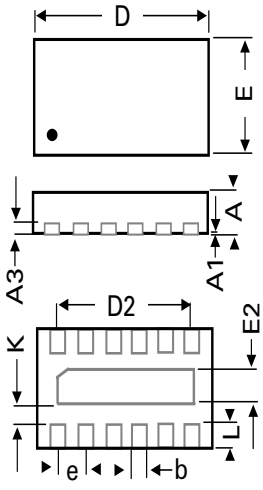
	UDFN-08			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.127 REF		0.005 REF	
b	0.150	0.250	0.006	0.010
D	1.600	1.800	0.063	0.071
D2	1.100	1.300	0.043	0.051
E	1.250	1.450	0.049	0.057
E2	0.300	0.500	0.012	0.020
e	0.400 BSC		0.016 BSC	
K	0.200		0.008	0.000
L	0.150	0.350	0.006	0.014

Package Dimensions — UDFN-16



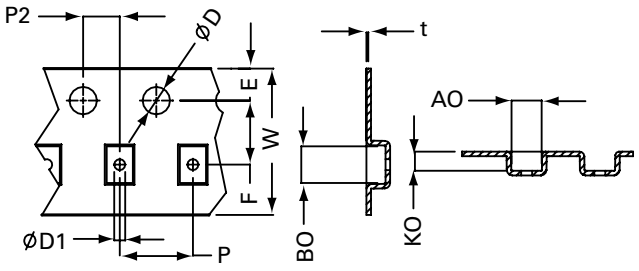
	UDFN-16			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.01	0.02
A1	0.00	0.05	0.00	0.002
A3	0.127 REF		0.00 REF	
b	0.15	0.25	0.00	0.00
D	3.20	3.40	0.12	0.13
D2	2.70	2.90	0.10	0.11
E	1.25	1.45	0.04	0.05
E2	0.30	0.50	0.01	0.01
e	0.40 BSC		0.01 BSC	
K	0.20		0.00	
L	0.15	0.35	0.00	0.01

Package Dimensions — UDFN-12



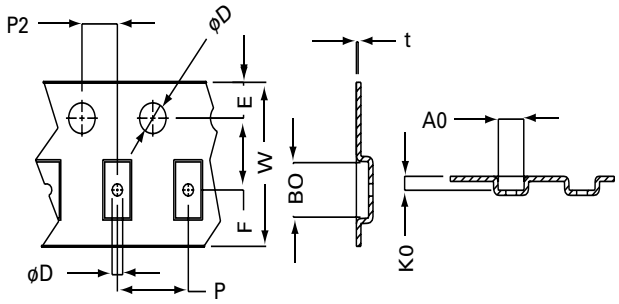
	UDFN-12			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.127 REF		0.005 REF	
b	0.150	0.250	0.006	0.010
D	2.400	2.600	0.094	0.102
D2	1.900	2.100	0.075	0.083
E	1.250	1.450	0.049	0.057
E2	0.300	0.500	0.012	0.020
e	0.400 BSC		0.016 BSC	
K	0.200		0.008	0.000
L	0.150	0.350	0.006	0.014

Embossed Carrier Tape & Reel Specification – UDFN-08



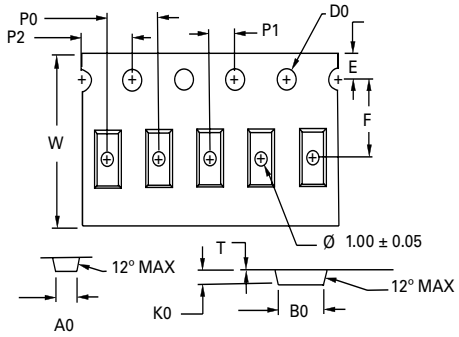
	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.136	0.140
D1	1.00	-	0.040	-
D	1.50 min		0.059 min	
P	3.90	4.10	0.154	0.161
10P	40.0 +/- 0.20		1.575 +/- 0.008	
W	7.70	8.30	0.303	0.327
P2	1.95	2.05	0.077	0.081
A0	1.55	1.75	0.061	0.069
B0	1.90	2.1	0.075	0.083
K0	0.95	1.15	0.037	0.045
t	0.30 max		0.012 max	

Embossed Carrier Tape & Reel Specification – UDFN-12



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.136	0.140
D1	0.55	0.65	0.021	0.025
D	1.50 min		0.059 min	
P	3.90	4.10	0.154	0.161
10P	40.0 +/- 0.20		1.575 +/- 0.008	
W	7.90	8.30	0.311	0.327
P2	1.95	2.05	0.077	0.081
A0	1.33	1.53	0.052	0.060
B0	2.63	2.83	0.103	0.111
K0	0.58	0.78	0.023	0.031
t	0.22 max		0.009 max	

Embossed Carrier Tape & Reel Specification – UDFN-16



	Millimetres		Inches	
	Min	Max	Min	Max
A0	1.55	1.75	0.06	0.06
B0	3.50	3.70	0.13	0.14
D0	1.40	1.60	0.05	0.06
E	1.65	1.85	0.06	0.07
F	5.45	5.55	0.21	0.21
K0	0.85	1.05	0.03	0.04
P0	3.90	4.10	0.15	0.16
P1	1.95	2.05	0.07	0.08
P2	3.90	4.10	0.15	0.16
T	0.26	0.30	0.01	0.01
W	11.90	12.30	0.46	0.48

Part Numbering System

SP 6001-0x U T G -1

- SP: Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- 6001: Series
- 0x: Number of Channels
  - 04 = 4 Channel UDFN-08
  - 06 = 6 Channel UDFN-12
  - 08 = 8 Channel UDFN-16
- U: Package
  - UDFN-08 (1.7x1.35mm)
  - UDFN-12 (2.5x1.35mm)
  - UDFN-16 (3.3x1.35mm)
- T: Tape & Reel
- G: Green
- -1

Part Marking System

JH4 / JH6 / JH8

J H x

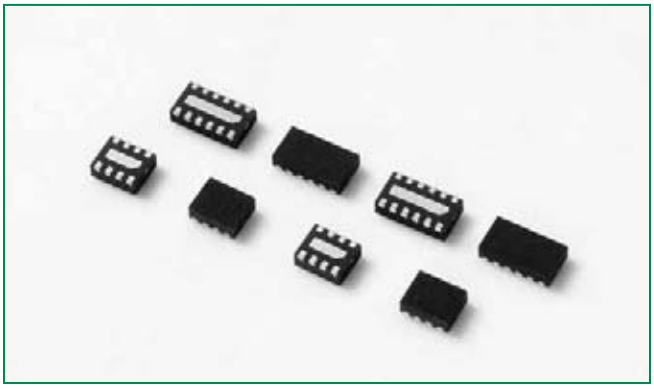
- J: Product Series, J = SP6001
- H: Assembly Site
- x:
  - 4 = UDFN-08
  - 6 = UDFN-12
  - 8 = UDFN-16

Ordering Information

Part Number	Package	Size (mm)	Marking	Min. Order Qty.
SP6001-04UTG-1	uDFN-08	1.7x1.35	JH4	3000
SP6001-06UTG-1	uDFN-12	2.5x1.35	JH6	3000
SP6001-08UTG-1	uDFN-16	3.3x1.35	JH8	3000

SP6002 Series 15pF 30kV EMI Filter Array

HF RoHS GREEN



Description

The Littelfuse SP6002 SPA series integrates 4 and 6 EMI filters (C-R-C) into a small, low-profile UDFN package with each filter providing greater than -30dB attenuation at 1GHz. Additionally, each I/O is capable of shunting ±30kV ESD strikes (IEC61000-4-2, contact discharge) away from sensitive electronic components. The performance of this small, slim design makes it extremely suitable for mobile handsets, PDAs and notebook computers.

Features

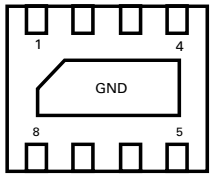
- EMI filtering of frequencies from 800MHz to 3GHz
- Greater than -30dB attenuation (TYP) at 1GHz
- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- Small, low-profile UDFN package (TYP 0.5mm height)

Applications

- Keypad interface for portable electronics
- LCD and camera display interfaces for handsets
- Connector interfaces for portable electronics
- Mobile phone
- Smartphone
- Portable navigation device

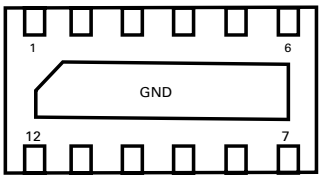
Pinout

UDFN-08



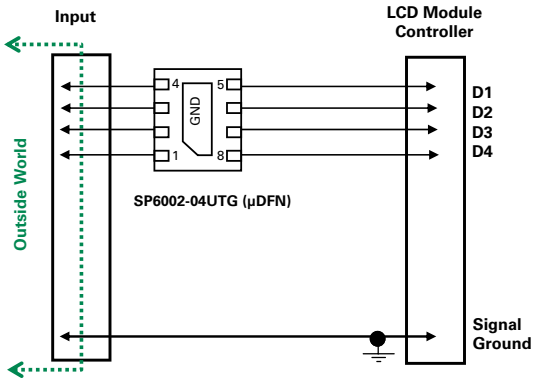
SP6002-04UTG-1

UDFN-12



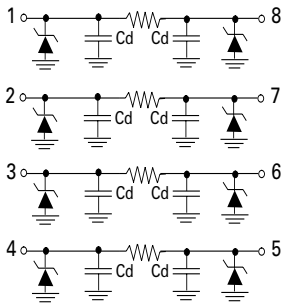
SP6002-06UTG-1

Application Example

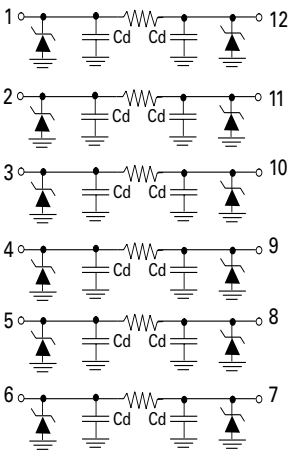


Functional Block Diagram

SP6002-04UTG-1



SP6002-06UTG-1



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

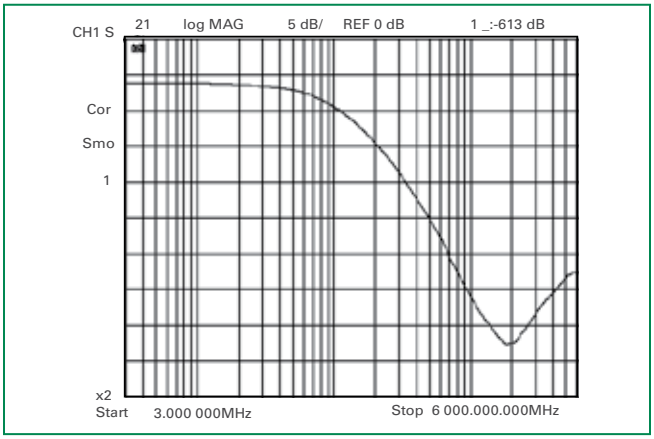
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics (T_{OP}=25°C)

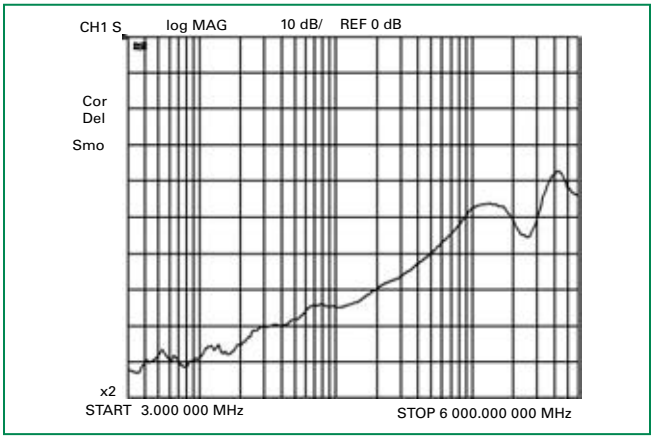
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}				6.0	V
Breakdown Voltage	V_{BR}	I_R=1mA	7.0	7.8	8.5	V
Reverse Leakage Current	I_{LEAK}	V_{RWM}=5V		0.1	1.0	µA
Resistance	R_A	I_R=10mA	85	100	115	Ω
Diode Capacitance[1,2]	C_D	V_R=2.5V,f=1MHz		15		pF
Line Capacitance[1,2]	C_L	V_R=2.5V,f=1MHz	24	30	36	pF
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact Discharge)	±30			kV
		IEC61000-4-2 (Air Discharge)	±30			kV
Cutoff Frequency[3]	F_{-3dB}	Above this frequency, appreciable attenuation occurs		100		MHz

Notes: [1] Parameter is guaranteed by design and/or device characterization.
[2] Total line capacitance is two times the diode capacitance (C_D).
[3] 50Ω source and 50Ω load termination

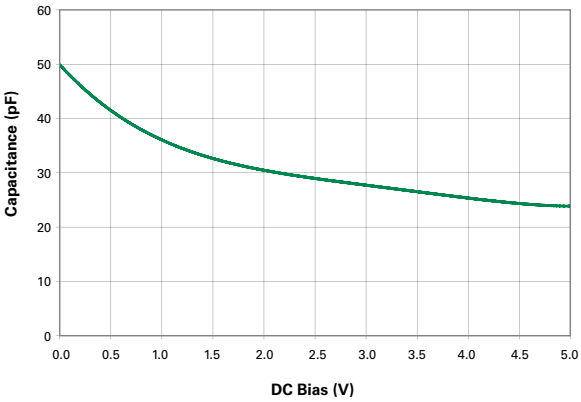
Insertion Loss (S21)



Analog Crosstalk (S41)



Line Capacitance vs. DC Bias



Product Characteristics

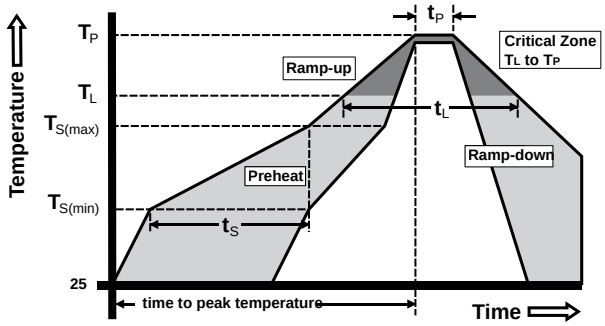
Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Part Numbering System

SP 6002-0x U T G -1

- SP 6002 — Silicon Protection Array (SPA™) Family of TVS Diode Arrays
- Series
- 0x — Number of Channels: 04 = 4 Channel UDFN-08; 06 = 6 Channel UDFN-12
- U — Package: UDFN-08 (1.7x1.35mm); UDFN-12 (2.5x1.35mm)
- T = Tape & Reel
- G = Green
- -1

Part Marking System

KH4
KH6

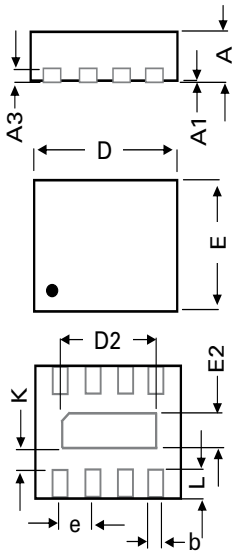
J H x

- J — Product Series: K = SP6002
- H — Assembly Site
- x — 4 = UDFN-08; 6 = UDFN-12

Ordering Information

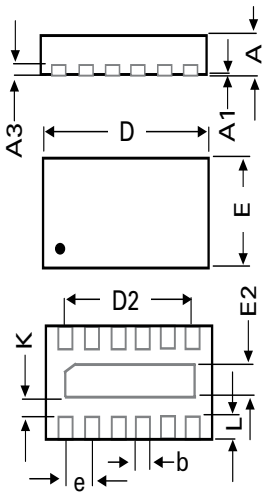
Part Number	Package	Size	Marking	Min. Order Qty.
SP6002-04UTG-1	uDFN-08	1.7x1.35mm	KH4	3000
SP6002-06UTG-1	uDFN-12	2.5x1.35mm	KH6	3000

Package Dimensions — UDFN-08



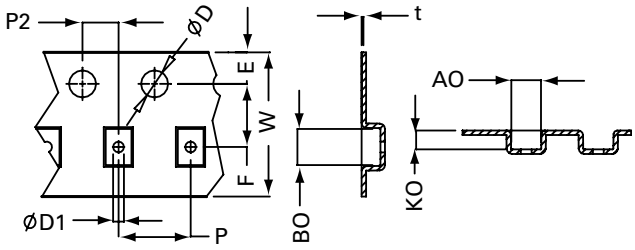
	UDFN-08			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
A3	0.127 REF		0.005 REF	
b	0.15	0.25	0.006	0.010
D	1.60	1.80	0.063	0.071
D2	1.10	1.30	0.043	0.051
E	1.25	1.45	0.049	0.057
E2	0.30	0.50	0.012	0.020
e	0.400 BSC		0.016 BSC	
K	0.20		0.008	0.000
L	0.15	0.35	0.006	0.014

Package Dimensions — UDFN-12



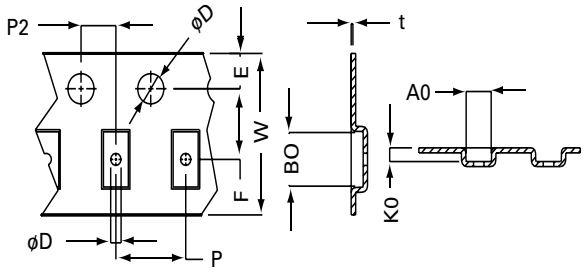
	UDFN-12			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
A3	0.127 REF		0.005 REF	
b	0.15	0.25	0.006	0.010
D	2.40	2.60	0.094	0.102
D2	1.90	2.10	0.075	0.083
E	1.25	1.45	0.049	0.057
E2	0.30	0.50	0.012	0.020
e	0.400 BSC		0.016 BSC	
K	0.20		0.008	0.000
L	0.15	0.35	0.006	0.014

Embossed Carrier Tape & Reel Specification – UDFN-08

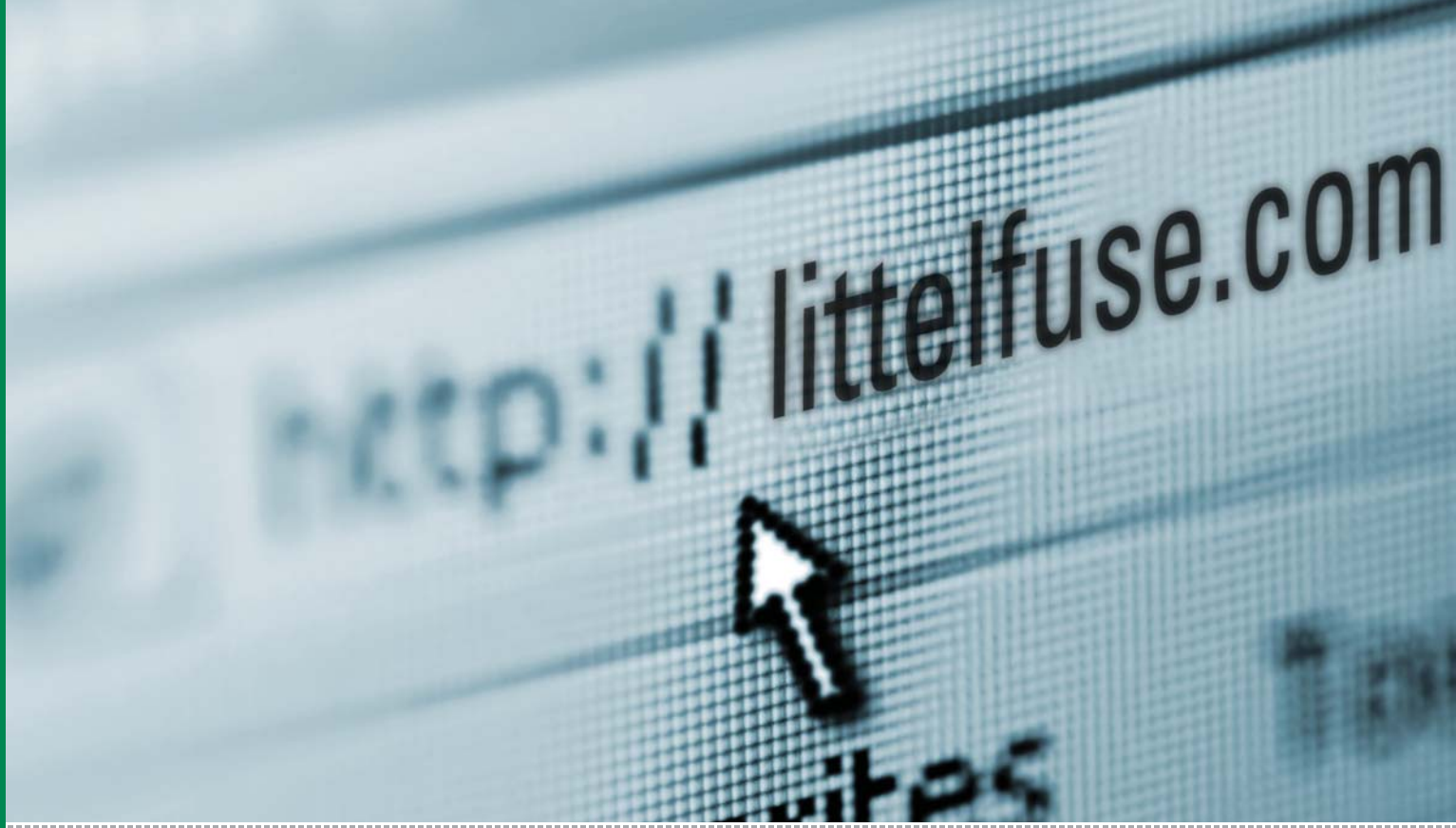


	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.136	0.140
D1	1.00	-	0.040	-
D	1.50 min		0.059 min	
P	3.90	4.10	0.154	0.161
10P	40.0 +/- 0.20		1.575 +/- 0.008	
W	7.70	8.30	0.303	0.327
P2	1.95	2.05	0.077	0.081
A0	1.55	1.75	0.061	0.069
B0	1.90	2.1	0.075	0.083
K0	0.95	1.15	0.037	0.045
t	0.30 max		0.012 max	

Embossed Carrier Tape & Reel Specification – UDFN-12



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.136	0.140
D1	0.55	0.65	0.021	0.025
D	1.50 min		0.059 min	
P	3.90	4.10	0.154	0.161
10P	40.0 +/- 0.20		1.575 +/- 0.008	
W	7.90	8.30	0.311	0.327
P2	1.95	2.05	0.077	0.081
A0	1.33	1.53	0.052	0.060
B0	2.63	2.83	0.103	0.111
K0	0.58	0.78	0.023	0.031
t	0.22 max		0.009 max	



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- > Reference Designs
- > Application Notes
- > Application Testing
- > SPICE Models
- > Local Technical Support
- > Product Samples
- > Technical Articles
- > Certification Documents
- > Data Sheets

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Overcurrent Protection Products:

Fuses Littelfuse offers the world's broadest range of fuse types and ratings, including cartridge, leaded, surface mount and thin film designs

PTCs Positive Temperature Coefficient thermistor technology provides resettable current-limiting protection

Protection Relays Electronic and microprocessor-based protection relays minimize damage to equipment and personnel caused by electrical faults

Overvoltage Protection Products:

Varistors Littelfuse offers surface mount Multi-Layer Varistors (MLVs) and industrial Metal Oxide Varistors (MOVs) to protect against transients

GDTs Gas Discharge Tubes (GDTs) to dissipate transient voltage through a contained plasma gas

Thyristors Solid state switches that control the flow of current in a wide range of appliances, tools and equipment

SIDACtor® Devices Overvoltage protection specifically designed for legacy telecom and today's broadband connections

TVS Diodes Silicon Transient Voltage Suppression (TVS) devices

SPA™ TVS Diode Arrays Silicon Protection Arrays (SPA) designed for analog and digital signal line protection

PulseGuard® ESD Suppressors Small, fast-acting Electrostatic Discharge (ESD) suppressors

Special Application Products:

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